

Compal Confidential

S530 (ELZ02) DIS M/B Schematics Document

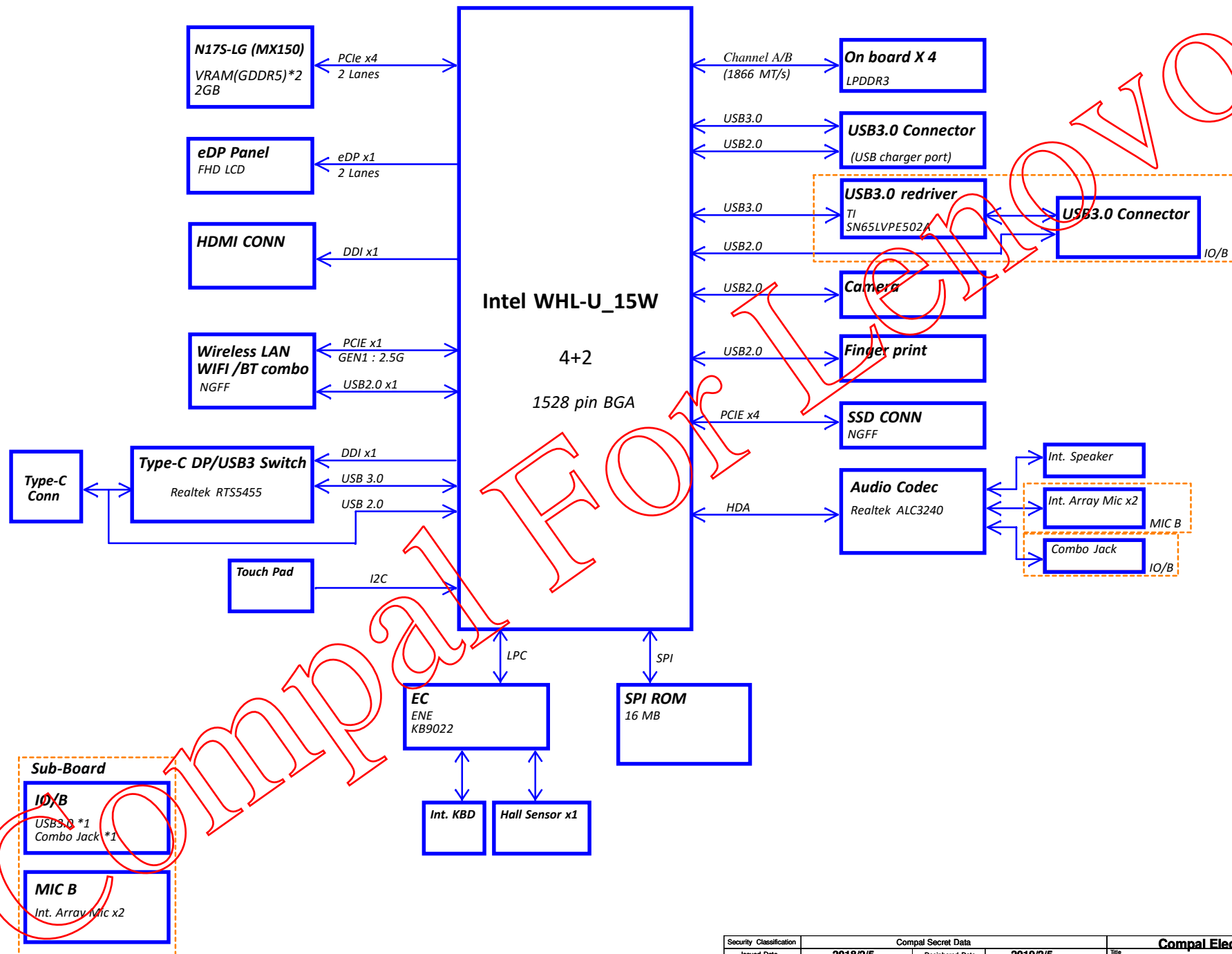
Intel Whiskey Lake U Processor with LPDDR3
N17S-LG (Geforce MX150) (23x23mm)

2018-5-21

LA-G651P

REV : 0 . 2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/2/5	Deciphered Date	2019/2/5	Title Cover Page	
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/2/5	Deciphered Date	2019/2/5	BLOCK DIAGRAM	
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Voltage Rails

power plane	State	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +VCCPLL_OC +VCCCORE +VCCGT +1.05V_VCCST +1.05VS_VCCIO +1.8VS +1.8V_MEM
S0		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

BOM Structure Table

Item	BOM Structure
For DIS	DIS@
For UMA	UMA@
For GPU GC6	GC6@
No GPU GC6	NOGC6@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For RF	RF@
No RF	@RF@
For EMI	EMI@
No EMI	@EMI@
For ESD	ESD@
No ESD	@ESD@
Connector	ME@
For Samsung VRAM	S2G@
For Micron VRAM	M2G@
For Hynix VRAM	H2G@
For samsung 4G DRAM	S4G@
For samsung 8G DRAM	S8G@
For samsung 16G DRAM	S16G@
For Hynix 4G DRAM	H4G@
For Hynix 8G DRAM	H8G@
For Hynix 16G DRAM	H16G@
For Micron 4G DRAM	M4G@
For Micron 8G DRAM	M8G@
For Micron 16G DRAM	M16G@
X4E for UMA	X4E_UMA
X4E for DIS	X4E_DIS
For CNVi interface	CNVi@
Non CNVi interface	NONCNVi@
For XDP	CMC@
For Thermal Sensor	EX_THM@
For 8G_16G DRAM	2774@

USB 2.0 Port Table

Port	
1	USB2/3 (re-driver) (I/O BD)
2	USB2/3 (Charger)
3	Type-C
4	
5	Camera
6	FP
7	
8	
9	
10	NGFF WLAN+BT(CNVi)

PCIe Port Table

Port	Lane	
1		
2		
3		
4		
5		
6		
7		
8		
9	3	NGFF WLAN+BT
10	2	
11	1	SSD
12	0	
13	0	
14	1	GPU
15	2	
16	3	

USB 3.0 Port Table

Port	
1	USB2/3 (re-driver) (I/O SB)
2	USB2/3 (for charger)
3	Type-C
4	
5	
6	

EMC/ESD	UMA	Discrete
	ZZZ X4E_UMA@ X4E_UMA X4EAD038L02	ZZZ X4E_DIS@ X4E_DIS X4EAD038L01

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	Thermal Sensor	Touch Pad	PCH	TypeC-Mux
EC_SMB_CK1 EC_SMB_DA1	KB9022QD +3VL	X	V	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB9022QD +3VS	V	X	X	Reserve	X	V	Reserve
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VS	X	X	X	X	X	X	X
I2C1_SCL_TS I2C1_SDA_TS	PCH +3VS	X	X	X	X	X	X	V
I2C0_SCL_TP I2C0_SDA_TP	PCH +3VS	X	X	X	X	V	X	X
Address	Write Read	0X9E			0X4C	0X2C		0X5C

CPU

ZZZ
DA801FP00
PCB 2D5 LA-G651P REV0 MB 2

MB

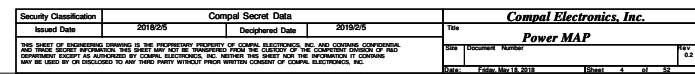
ZZZ 45@
HDMI Logo
RC000000SRM

HDMI Logo

LPDDR3 Onboard RAM

	LPDDR3_S4G	LPDDR3_H4G	LPDDR3_M4G
4G	ZZZ X76@ LPDDR3_S4G X7679138L01	ZZZ X76@ LPDDR3_H4G X7679138L02	ZZZ X76@ LPDDR3_M4G X7679138L03
8G	ZZZ X76@ LPDDR3_S8G X7679138L04	ZZZ X76@ LPDDR3_H8G X7679138L05	ZZZ X76@ LPDDR3_M8G X7679138L06
16G	ZZZ X76@ LPDDR3_S16G X7679138L07	ZZZ X76@ LPDDR3_H16G X7679138L08	ZZZ X76@ LPDDR3_M16G X7679138L09

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Issued Date	2018/2/5	Deciphered Date	2019/2/5	Notes List
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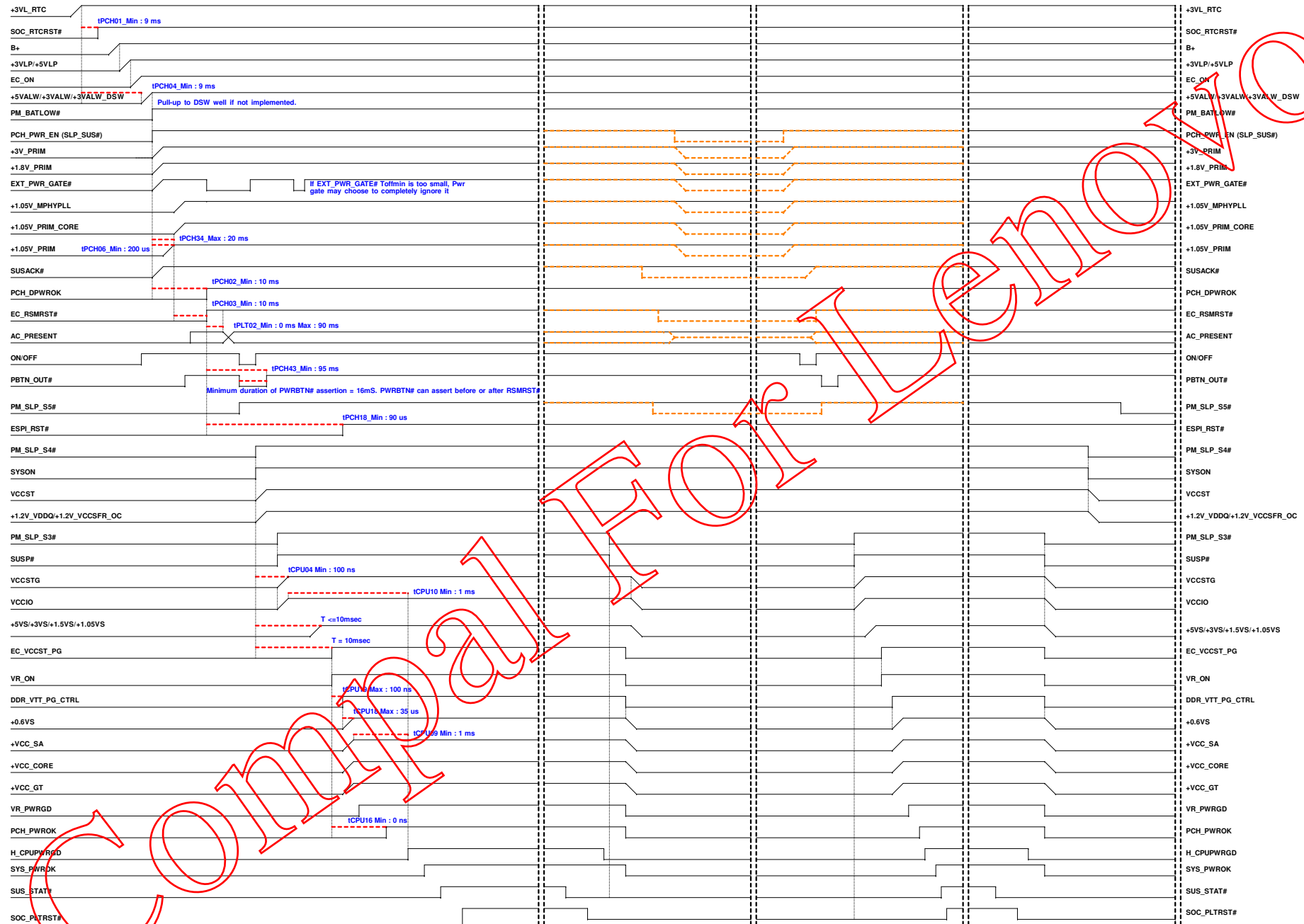


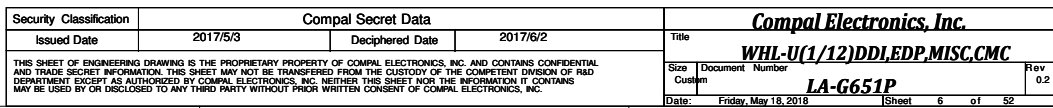
G3→S0

S0→S3/DS3

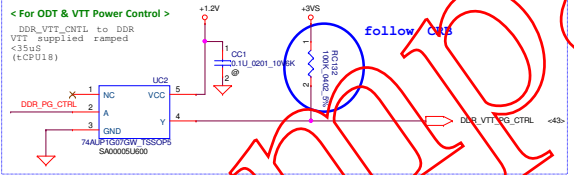
S0/DS3→S0

S0→S5





Non- Interleaved Memory



Security Classification		Compal Secret Data		Title	
Issued Date	2018/02/06	Deciphered Date	2020/5/17	Doc Number	WHL-U(2/12)LPDDR3
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Note:

The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

SML1ALERT#/
PCHHOT#/GPP_B23

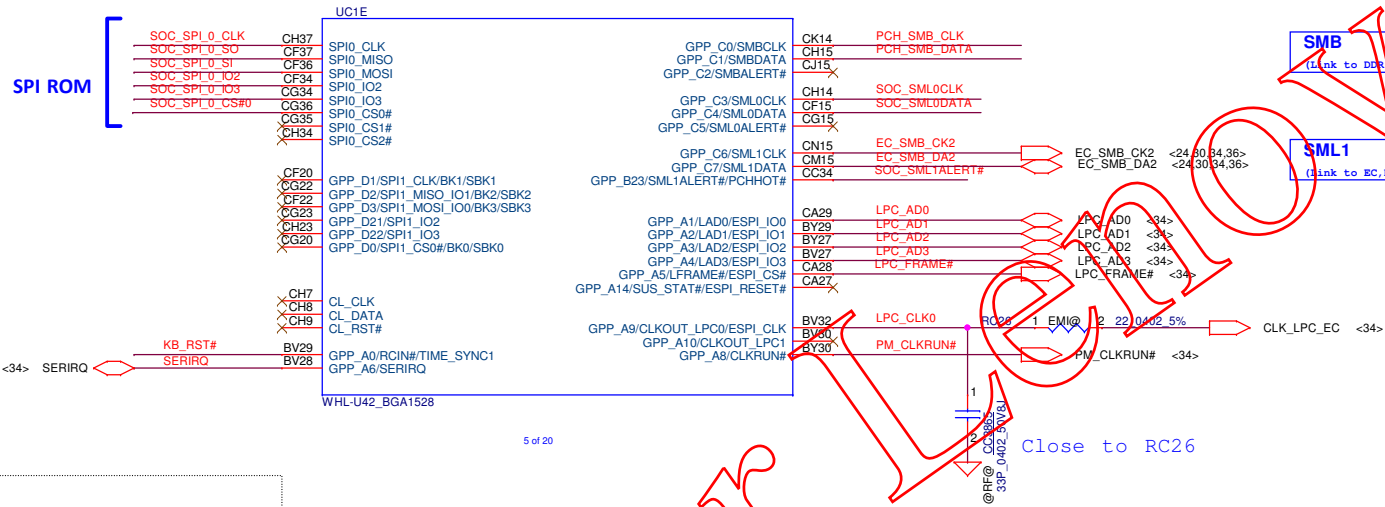
- If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.
- If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.
- If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor]

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

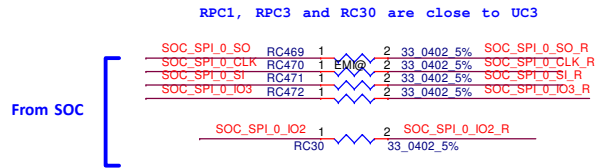
1 = eSPI is selected for EC



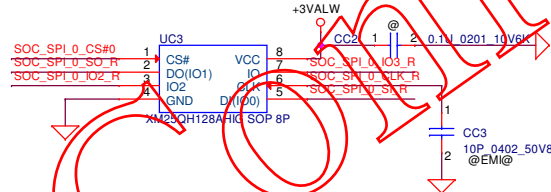
SMB
(link to DPA)

SML1
(link to EC, DGPU, Thermal IC)

Close to RC26



< SPI ROM - 16M >



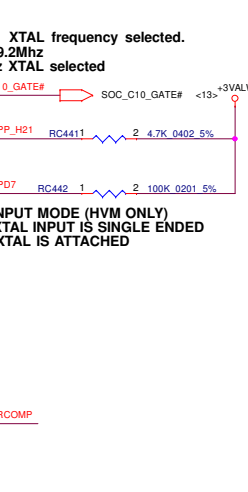
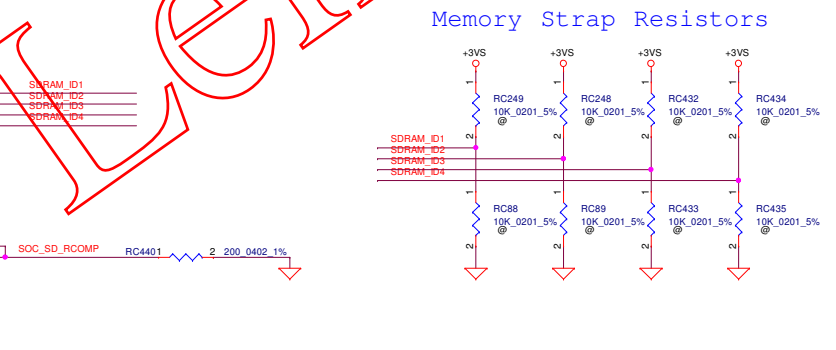
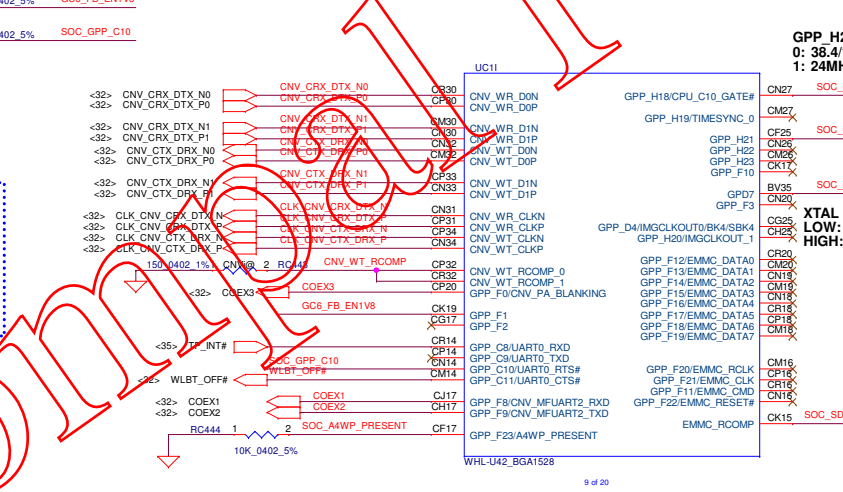
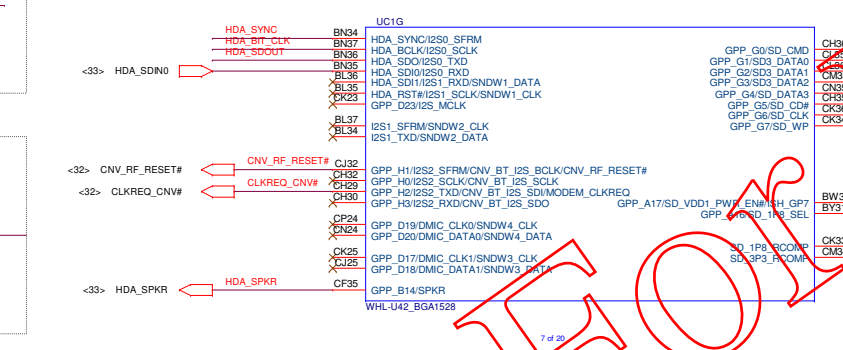
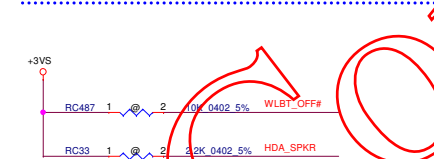
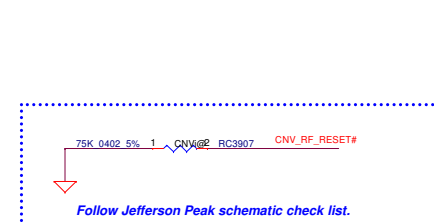
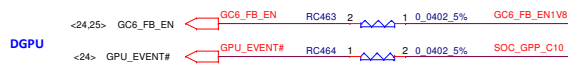
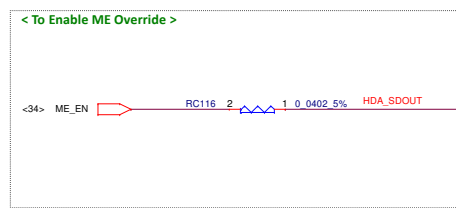
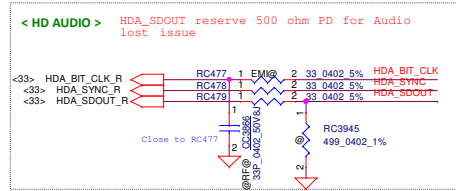
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Issued Date	2017/5/3	Deciphered Date	2017/6/2	Title	WHL-U(3/12)SPI,SMB,LPC,ESPI
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CPU Memory down vender control table

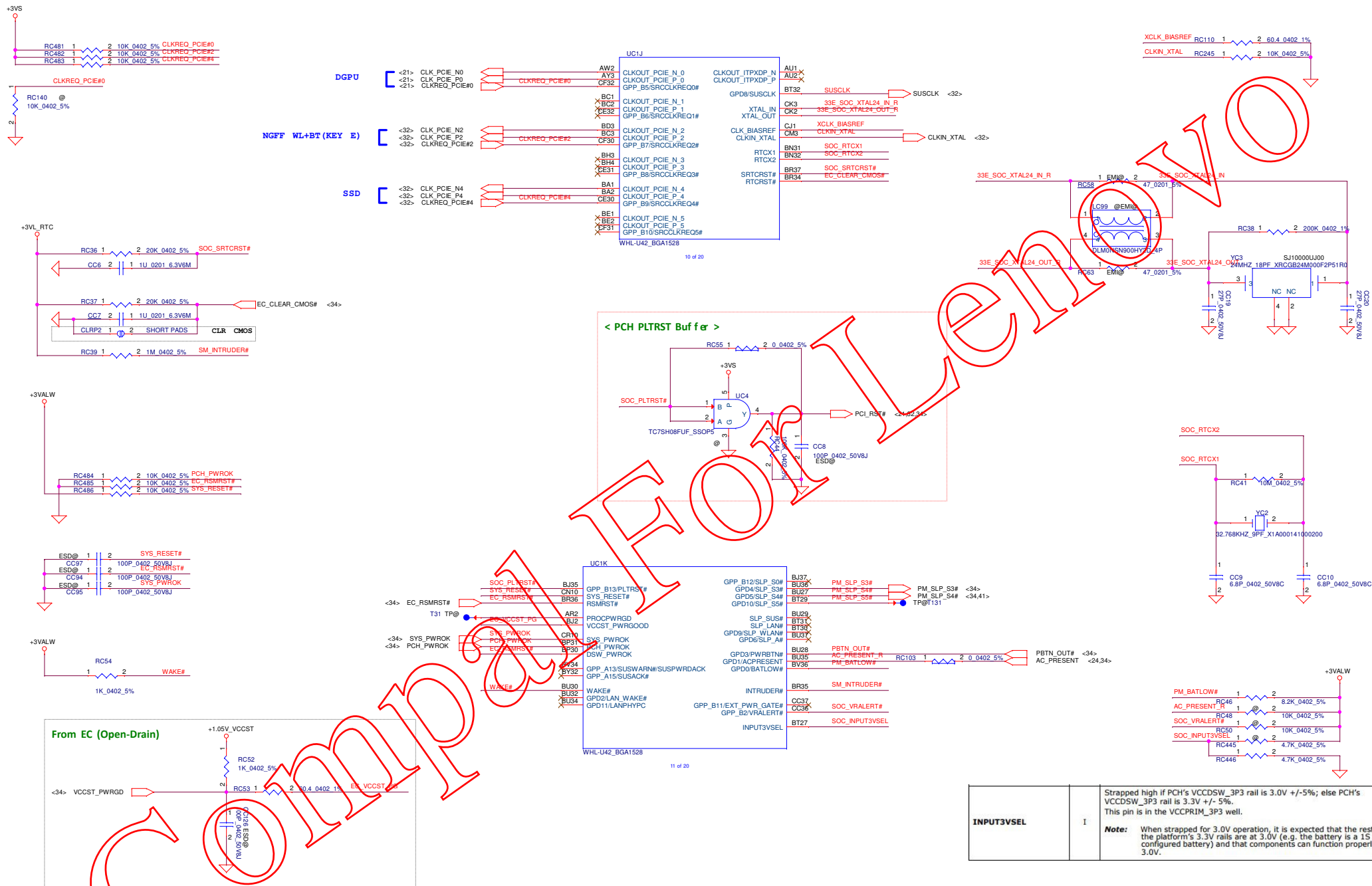
CPU_GPP_G7	CPU_GPP_G6	Vender	CPU_GPP_G5	CPU_GPP_G4	MD size	Vender description
SDRAM_ID4	SDRAM_ID3		SDRAM_ID2	SDRAM_ID1		
0	0	Samsung	0	0	4GB	K4E8E324EB-EGCG
			0	1	8GB	K4E6E304EC-EGCG
			1	0	16GB	K4E6E304EC-EGCG
			1	1	4GB	K4E6E304EC-EGCG(CHB-ONLY)
0	1	Hynix	0	0	4GB	H9CCNNN8GTALAR-NVD
			0	1	8GB	H9CCNNNBJTALAR-NVD
			1	0	16GB	H9CCNNNCLGALAR-NVD
			1	1	4GB	H9CCNNNBJTALAR-NVD(CHB-ONLY)
1	0	Micron	0	0	4GB	MT52L256M32D1PF-093WT:B
			0	1	8GB	MT52L512M32D2PF-093WT:B
			1	0	16GB	MT52L1G32D4PG-093WT:B
			1	1	4GB	MT52L512M32D2PF-093WT:B(CHB-ONLY)

BOM Conf i g

Vender	MD size	SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	LPDDR3			
Samsung	4GB	RC435 S4G@	RC433 S4G@	RC248 S4G@	RC249 S4G@	UD3 S4G@ SA0000AZT20	UD4 S4G@ SA0000AZT20		
	8GB	RC435 S8G@	RC433 S8G@	RC89 S8G@	RC249 S8G@	UD1 S8G@ SA0000AZT20	UD2 S8G@ SA0000AZT20	UD3 S8G@ SA0000AZT20	UD4 S8G@ SA0000AZT20
	16GB	RC435 S16G@	RC433 S16G@	RC248 S16G@	RC88 S16G@	UD1 S16G@ SA00008V20	UD2 S16G@ SA00008V20	UD3 S16G@ SA00008V20	UD4 S16G@ SA00008V20
	4GB	RC435 H4G@	RC432 H4G@	RC248 H4G@	RC249 H4G@	UD3 H4G@ SA0000ALP00	UD4 H4G@ SA0000ALP00		
Hynix	8GB	RC435 H8G@	RC432 H8G@	RC89 H8G@	RC249 H8G@	UD1 H8G@ SA0000ALP00	UD2 H8G@ SA0000ALP00	UD3 H8G@ SA0000ALP00	UD4 H8G@ SA0000ALP00
	16GB	RC435 H16G@	RC432 H16G@	RC248 H16G@	RC88 H16G@	UD1 H16G@ SA00009ZL00	UD2 H16G@ SA00009ZL00	UD3 H16G@ SA00009ZL00	UD4 H16G@ SA00009ZL00
	4GB	RC434 M4G@	RC433 M4G@	RC248 M4G@	RC249 M4G@	UD3 M4G@ SA0000AM400	UD4 M4G@ SA0000AM400		
	8GB	RC434 M8G@	RC433 M8G@	RC89 M8G@	RC249 M8G@	UD1 M8G@ SA0000AM400	UD2 M8G@ SA0000AM400	UD3 M8G@ SA0000AM400	UD4 M8G@ SA0000AM400
Micron	16GB	RC434 M16G@	RC433 M16G@	RC88 M16G@	RC88 M16G@	UD1 M16G@ SA00009ZN00	UD2 M16G@ SA00009ZN00	UD3 M16G@ SA00009ZN00	UD4 M16G@ SA00009ZN00



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NGFF WLAN+BT

SSD

dGPU

Near UC1

UC1H

BW9
BW8
BW4
BW3

BU6
BU5
BU4
BU3

BT7
BT6
BT2
BT1

BU9
BU8
BT4
BT3

BP5
BP6
BR2
BR1

BN6
BN5
BR4
BR3

BN10
BN8
BN4
BN3

BL6
BL5
BN2
BN1

BK6
BK5
BM4
BM3

BJ6
BJ5
BL2
BL1

BC5
BC6
BL4
BL3

BE5
BE6
BJ4
BJ3

CE6
CE5

CR28
CP28
CN28
CM28

WHL-U42_BGA1528

PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP
PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP

PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP

PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP

PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

PCIE10_RXN
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PCIE10_TXN
PCIE10_TXP

PCIE11_RXN/SATA0_RXN
PCIE11_RXP/SATA0_RXP
PCIE11_TXN/SATA0_TXN
PCIE11_TXP/SATA0_TXP

PCIE12_RXN/SATA1A_RXN
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PCIE12_TXP/SATA1A_TXP

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PCIE13_TXP

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PCIE14_TXN
PCIE14_TXP

PCIE15_RXN/SATA1B_RXN
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PCIE15_TXN/SATA1B_TXN
PCIE15_TXP/SATA1B_TXP

PCIE16_RXN/SATA2_RXN
PCIE16_RXP/SATA2_RXP
PCIE16_TXN/SATA2_TXN
PCIE16_TXP/SATA2_TXP

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PCIE3_RXN/USB31_3_RXN
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PCIE3_TXP/USB31_3_TXP

PCIE4_RXN/USB31_4_RXN
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PCIE4_TXN/USB31_4_TXN
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USB2_1N
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USB2_2P

USB2_3N
USB2_3P
USB2_4N
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USB2_6N
USB2_6P

USB2_7N
USB2_7P
USB2_8N
USB2_8P

USB2_9N
USB2_9P
USB2_10N
USB2_10P

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E9/USB2_OC0#/GP_BSSB_CLK
GPP_E10/USB2_OC1#/GP_BSSB_D1
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

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GPP_E1/SATA1PCIE1/SATAGP1
GPP_E2/SATA1PCIE2/SATAGP2

GPP_E8/SATALED#/SPI_CS1#
UFS_RESET#

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

CB5
CB6
CA4
CA3

BY8
BY9
CA2
CA1

BY7
BY6
BY4
BY3

BW6
BW5
BW2
BW1

CE3
CE4

CE1
CE2

CG3
CG4

CD3
CD4

CG5
CG6

CC1
CC2

CG8
CG9

CH5
CH6

CC3
CC4

CC5
CC8
CC6

CK6
CK5
CK8
CK9

CP8
CP8
CM8

CM8
CM10
CP10

CN7
AR3

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

USB3_CRX_DTX_N1
USB3_CRX_DTX_P1
USB3_CTX_DRX_N1
USB3_CTX_DRX_P1

USB3_CRX_DTX_N2
USB3_CRX_DTX_P2
USB3_CTX_DRX_N2
USB3_CTX_DRX_P2

USB3_CRX_MTX_N3
USB3_CRX_MTX_P3
USB3_CTX_MTX_N3
USB3_CTX_MTX_P3

USB20_N1
USB20_P1

USB20_N2
USB20_P2

USB20_N3
USB20_P3

USB20_N5
USB20_P5

USB20_N6
USB20_P6

USB20_N10
USB20_P10

USB2_COMP
USB2_ID
USB2_VBUSSENSE

USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

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WHL-U42_BGA1528

WHL-U42_BGA1528

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WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

WHL-U42_BGA1528

USB2/3 (re-driver) (I/O SB)

USB2/3 (for charger)

Type-C

USB2/3 (re-driver) (I/O BD)

USB2/3 (Charger)

Type-C

Camera

FP

CNVi

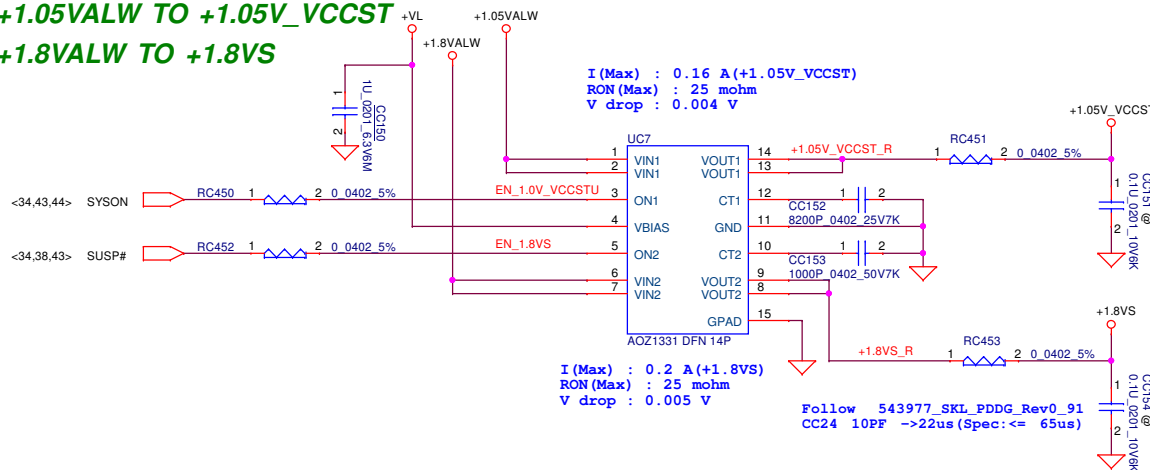
Trace length max: 450mils

USB_OC2# RC490 2 1 10K 0402 5%
USB_OC0# RC491 2 1 10K 0402 5%
USB_OC3# RC492 2 1 10K 0402 5%
USB_OC1# RC493 2 1 10K 0402 5%

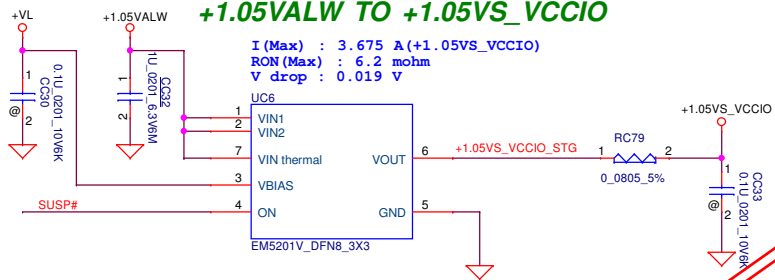
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Issued Date	2017/5/3	Deciphered Date	2017/6/2	Compal Electronics, Inc.	
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				Custom	LA-G651P
Date:		Friday, May 18, 2018		Sheet	12 of 52

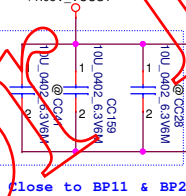
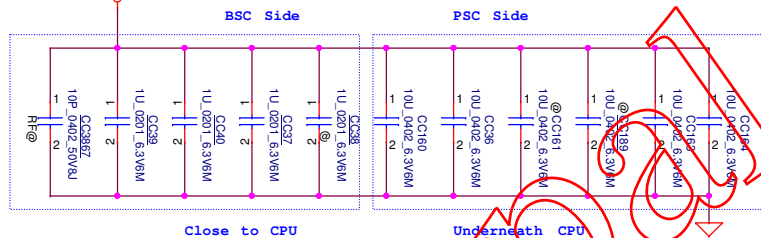
+1.05VALW TO +1.05V_VCCST
+1.8VALW TO +1.8VS



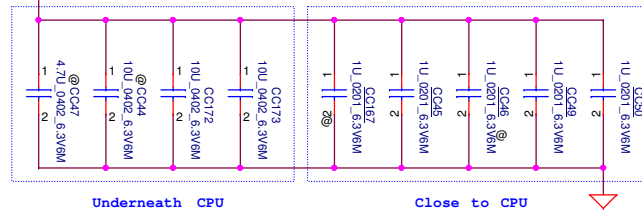
+1.05VALW TO +1.05VS_VCCIO



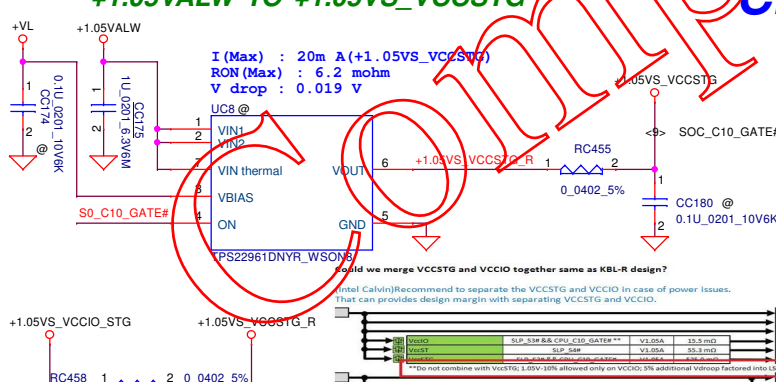
change package of 1U from 0201 to 0402



change package of 1U from 0201 to 0402

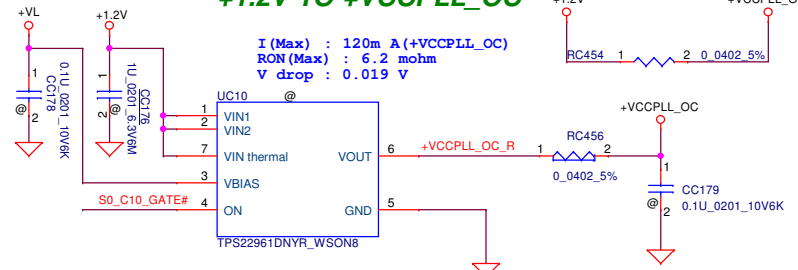


+1.05VALW TO +1.05VS_VCCSTG



CPU C10 Save Power

+1.2V TO +VCCPLL_OC



Could we merge VCCSTG and VCCIO together same as KBL-R design?

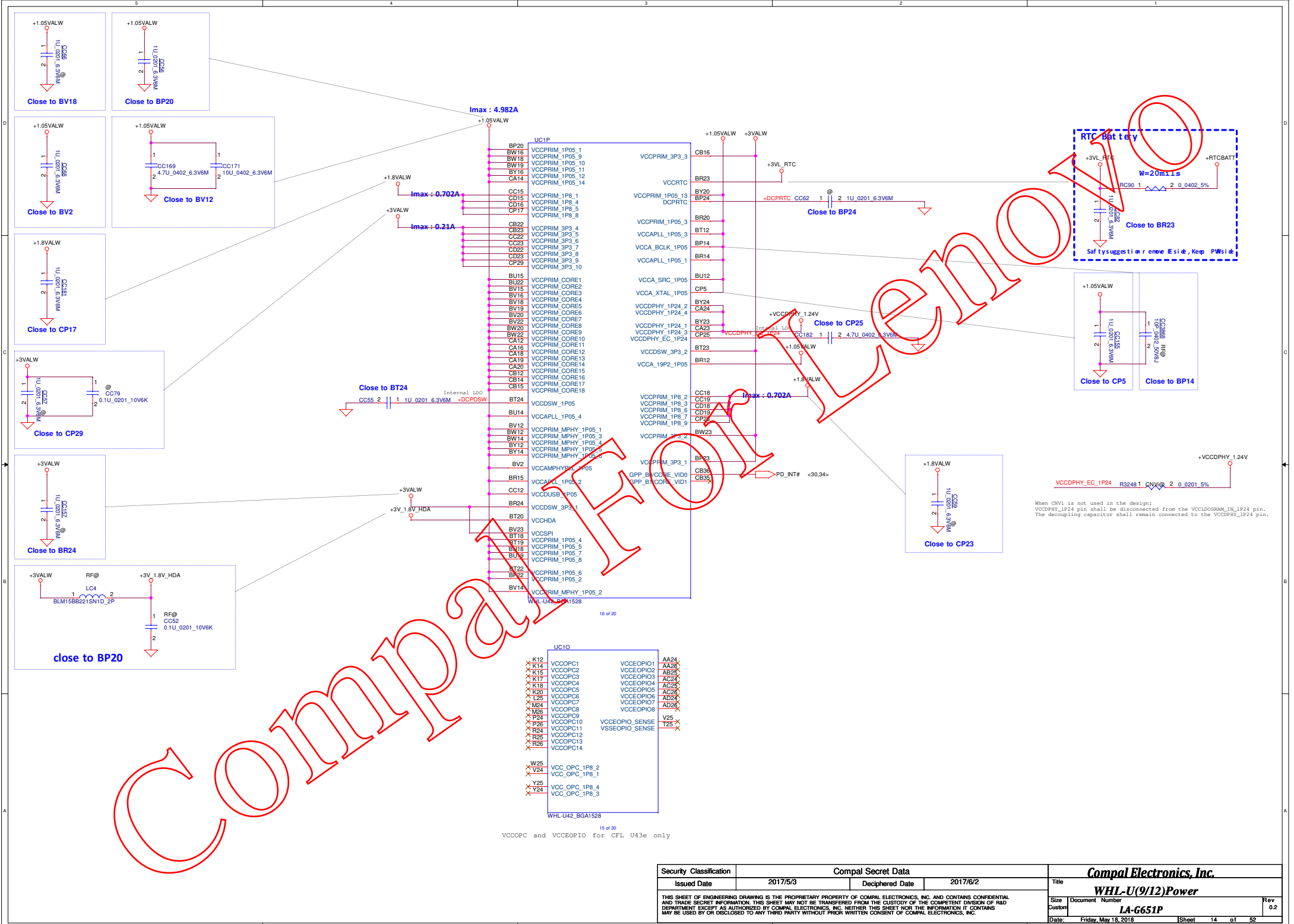
(Intel Calvin)Recommend to separate the VCCSTG and VCCIO in case of power issues. That can provides design margin with separating VCCSTG and VCCIO.

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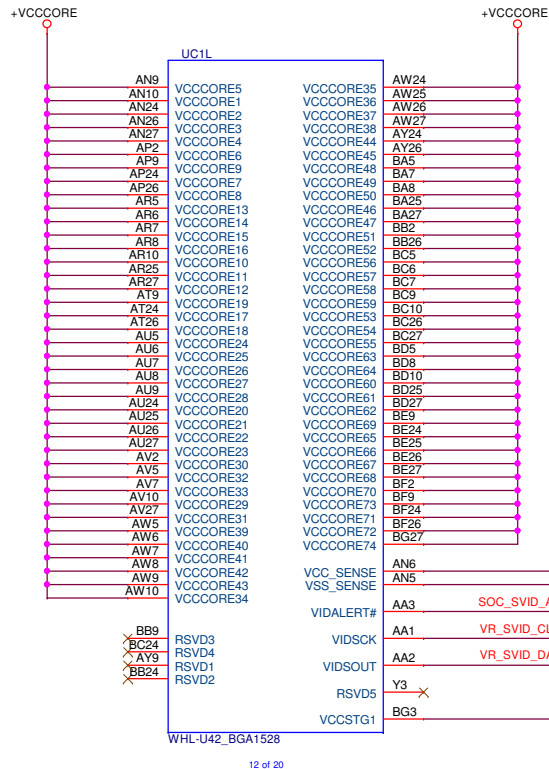
Compal Electronics, Inc.

WHL-U(8/12)Power

Size	Document Number	Rev
Custom	LA-G651P	0.2
Date:	Friday, May 18, 2018	Sheet 13 of 52

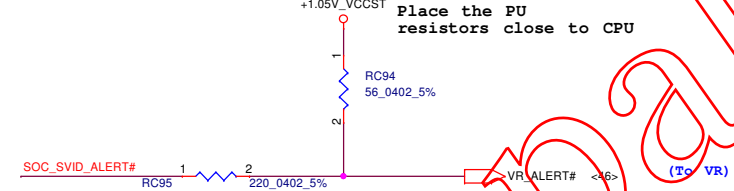


Security Classification		Compal Secret Data		Title	
Issued Date	2017/5/3	Deciphered Date	2017/6/2	WHL-U(9/12)Power	
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				Date	Friday, May 18, 2018
				Sheet	14 of 52

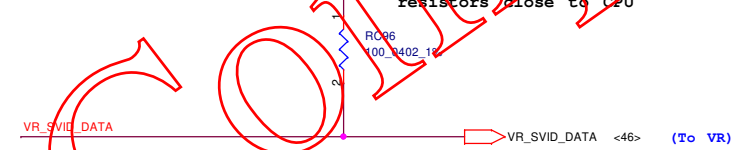


Pin Number	WHL U42 QS/Production	CNL U22/WHL-U42 ESO
AA9	VCCCORE	VCCGT
AB10	VCCCORE	VCCGT
AB2	VCCCORE	VCCGT
AB8	VCCCORE	VCCGT
AB9	VCCCORE	VCCGT
AC2	VCCCORE	VCCGT
AD9	VCCCORE	VCCGT
AE10	VCCCORE	VCCGT
AE8	VCCCORE	VCCGT
AE9	VCCCORE	VCCGT
AF10	VCCCORE	VCCGT
AF2	VCCCORE	VCCGT
AF8	VCCCORE	VCCGT
AG8	VCCCORE	VCCGT
AG9	VCCCORE	VCCGT
AH9	VCCCORE	VCCGT
AJ10	VCCCORE	VCCGT
AJ8	VCCCORE	VCCGT
AK2	VCCCORE	VCCGT
AK9	VCCCORE	VCCGT
AL10	VCCCORE	VCCGT
AL8	VCCCORE	VCCGT
AL9	VCCCORE	VCCGT
AM8	VCCCORE	VCCGT
Y2	VCCCORE	VCCGT
Y10	VCCCORE	VCCGT
Y8	VCCCORE	VCCGT

SVID ALERT



SVID DATA



UC1R			
CR34	VSS_1	VSS_73	BL7
BT5	VSS_2	VSS_74	AE25
BY5	VSS_3	VSS_75	BM33
CP35	VSS_4	VSS_76	CM5
CM37	VSS_5	VSS_77	AE27
CK37	VSS_6	VSS_78	BM35
AW1	VSS_7	VSS_79	CM9
CM1	VSS_8	VSS_80	AE30
BD6	VSS_9	VSS_81	BM36
AY4	VSS_10	VSS_82	CM13
B34	VSS_11	VSS_83	AE7
E35	VSS_12	VSS_84	BM9
A4	VSS_13	VSS_85	CM17
AE24	VSS_14	VSS_86	AF27
AE26	VSS_15	VSS_87	BN30
AF25	VSS_16	VSS_88	CM21
AG24	VSS_17	VSS_89	AF3
AG26	VSS_18	VSS_90	BN7
AH24	VSS_19	VSS_91	CM25
AH25	VSS_20	VSS_92	AF30
B2	VSS_21	VSS_93	CM29
B36	VSS_22	VSS_94	AF33
C36	VSS_23	VSS_95	BP15
C37	VSS_24	VSS_96	AF36
CM1	VSS_25	VSS_97	AF4
CM2	VSS_26	VSS_98	CM5
CM37	VSS_27	VSS_99	AF7
CP2	VSS_28	VSS_100	BP25
D1	VSS_29	VSS_101	AG10
A32	VSS_30	VSS_102	BP3
F33	VSS_31	VSS_103	CP1
A3	VSS_32	VSS_104	BP32
BJ7	VSS_33	VSS_105	CP11
CJ36	VSS_34	VSS_106	AF27
A36	VSS_35	VSS_107	BP33
BK10	VSS_36	VSS_108	CP13
CJ4	VSS_37	VSS_109	AH28
AB27	VSS_38	VSS_110	BP4
BK2	VSS_39	VSS_111	CP15
CK1	VSS_40	VSS_112	AH29
AB3	VSS_41	VSS_113	BP7
BK28	VSS_42	VSS_114	CP19
AB30	VSS_43	VSS_115	AH30
BK3	VSS_44	VSS_116	CP21
CK4	VSS_45	VSS_117	AH31
AB33	VSS_46	VSS_118	BR19
BK33	VSS_47	VSS_119	CP27
CK7	VSS_48	VSS_120	AH33
AB36	VSS_49	VSS_121	BR25
BK4	VSS_50	VSS_122	AH35
CL2	VSS_51	VSS_123	CP37
AB4	VSS_52	VSS_124	AJ25
BK7	VSS_53	VSS_125	BT15
CM13	VSS_54	VSS_126	AJ28
AB7	VSS_55	VSS_127	BT16
BL25	VSS_56	VSS_128	CP9
CM17	VSS_57	VSS_129	AJ7
AC10	VSS_58	VSS_130	CR2
BL28	VSS_59	VSS_131	AK3
CM21	VSS_60	VSS_132	CR36
AC27	VSS_61	VSS_133	AK33
BL29	VSS_62	VSS_134	D21
CM25	VSS_63	VSS_135	AK36
AC30	VSS_64	VSS_136	BT25
BL30	VSS_65	VSS_137	D25
CM29	VSS_66	VSS_138	AK4
BL31	VSS_67	VSS_139	BT26
CM31	VSS_68	VSS_140	AK2
AD33	VSS_69	VSS_141	BT33
BL32	VSS_70	VSS_142	D5
CM33	VSS_71	VSS_143	AL29
AD35	VSS_72	VSS_144	

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UC1S			
BT35	VSS_145	VSS_217	BY25
AL32	VSS_146	VSS_218	J18
BT36	VSS_147	VSS_219	AU32
D8	VSS_148	VSS_220	J21
AL7	VSS_149	VSS_221	AV25
D9	VSS_150	VSS_222	BY33
AM10	VSS_151	VSS_223	J24
BU11	VSS_152	VSS_224	AV28
E23	VSS_153	VSS_225	BY35
AM28	VSS_154	VSS_226	J33
E27	VSS_155	VSS_227	AV3
AM33	VSS_156	VSS_228	BY36
BU23	VSS_157	VSS_229	J36
E29	VSS_158	VSS_230	AV33
AM35	VSS_159	VSS_231	J6
BU24	VSS_160	VSS_232	AV36
E31	VSS_161	VSS_233	C1
BU25	VSS_162	VSS_234	K21
E33	VSS_163	VSS_235	AV4
AN25	VSS_164	VSS_236	C21
BU7	VSS_165	VSS_237	K22
E9	VSS_166	VSS_238	AV6
AN28	VSS_167	VSS_239	C25
BY11	VSS_168	VSS_240	K24
F12	VSS_169	VSS_241	AV8
AN29	VSS_170	VSS_242	C29
F15	VSS_171	VSS_243	K25
AN30	VSS_172	VSS_244	AW28
CM9	VSS_173	VSS_245	K27
AN31	VSS_174	VSS_246	AW29
BY3	VSS_175	VSS_247	C4
F2	VSS_176	VSS_248	K28
AN7	VSS_177	VSS_249	AW3
BY31	VSS_178	VSS_250	C2
F21	VSS_179	VSS_251	K29
AN8	VSS_180	VSS_252	AW30
BY33	VSS_181	VSS_253	K3
F24	VSS_182	VSS_254	CA11
BY4	VSS_183	VSS_255	K3
F3	VSS_184	VSS_256	AW31
AN9	VSS_185	VSS_257	CA15
AW11	VSS_186	VSS_258	K30
F4	VSS_187	VSS_259	CA22
AP33	VSS_188	VSS_260	K31
BY15	VSS_189	VSS_261	AY35
G21	VSS_190	VSS_262	K32
AP36	VSS_191	VSS_263	B12
G27	VSS_192	VSS_264	K4
AP4	VSS_193	VSS_265	B15
G33	VSS_194	VSS_266	CA25
AR28	VSS_195	VSS_267	K9
G35	VSS_196	VSS_268	B18
G36	VSS_197	VSS_269	CB11
AT33	VSS_198	VSS_270	L27
BY24	VSS_199	VSS_271	B21
G9	VSS_200	VSS_272	L33
AT35	VSS_201	VSS_273	B23
H21	VSS_202	VSS_274	L35
AT36	VSS_203	VSS_275	B25
BY7	VSS_204	VSS_276	CB18
H27	VSS_205	VSS_277	L36
AK33	VSS_206	VSS_278	B27
BY11	VSS_207	VSS_279	CB19
AU10	VSS_208	VSS_280	B29
BY15	VSS_209	VSS_281	CB2
H9	VSS_210	VSS_282	N25
AU28	VSS_211	VSS_283	B31
BY22	VSS_212	VSS_284	CB20
AD26	VSS_213	VSS_285	N27
AU29	VSS_214	VSS_286	CB25
J15	VSS_215	VSS_287	
	VSS_216	VSS_288	
		VSS_289	

WHL-U42_BGA1528

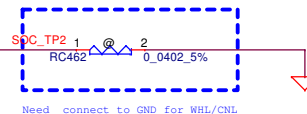
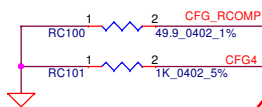
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UC1T			
N6	VSS_290	VSS_362	CF23
B37	VSS_291	VSS_363	CF24
CB3	VSS_292	VSS_364	CF28
P10	VSS_293	VSS_365	W10
B5	VSS_294	VSS_366	BE3
CB33	VSS_295	VSS_367	CF3
P3	VSS_296	VSS_368	W3
B7	VSS_297	VSS_369	CF4
CB4	VSS_298	VSS_370	W31
P33	VSS_299	VSS_371	BF3
B9	VSS_300	VSS_372	CF33
CB36	VSS_301	VSS_373	W33
P36	VSS_302	VSS_374	CF36
BA10	VSS_303	VSS_375	BF33
CB11	VSS_304	VSS_376	BF36
BA38	VSS_305	VSS_377	Y26
P3	VSS_306	VSS_378	BF4
BA3	VSS_307	VSS_379	CH31
CB20	VSS_308	VSS_380	Y27
CB25	VSS_309	VSS_381	BG25
R27	VSS_310	VSS_382	Y30
BB3	VSS_311	VSS_383	CB28
CB25	VSS_312	VSS_384	CJ11
R28	VSS_313	VSS_385	Y33
BB33	VSS_314	VSS_386	CJ14
CC28	VSS_315	VSS_387	Y35
R29	VSS_316	VSS_388	BH28
BB36	VSS_317	VSS_389	CJ19
CC31	VSS_318	VSS_390	Y7
R30	VSS_319	VSS_391	BH29
BB4	VSS_320	VSS_392	CJ23
CC7	VSS_321	VSS_393	BH32
R31	VSS_322	VSS_394	CJ26
BC25	VSS_323	VSS_395	BH33
CD11	VSS_324	VSS_396	CJ33
T27	VSS_325	VSS_397	BH35
CD12	VSS_326	VSS_398	CJ35
T30	VSS_327	VSS_399	BP19
BC29	VSS_328	VSS_400	BR16
CD14	VSS_329	VSS_401	BY18
T33	VSS_330	VSS_402	BY19
T35	VSS_331	VSS_403	CC16
BC32	VSS_332	VSS_404	BU16
CD24	VSS_333	VSS_405	CC14
T36	VSS_334	VSS_406	BR22
CD25	VSS_335	VSS_407	BU20
T7	VSS_336	VSS_408	CD20
BC8	VSS_337	VSS_409	BT14
CE33	VSS_338	VSS_410	BP12
U26	VSS_339	VSS_411	CB24
BD28	VSS_340	VSS_412	CC24
CE35	VSS_341	VSS_413	J5
U7	VSS_342	VSS_414	U24
BD33	VSS_343	VSS_415	BD7
CE36	VSS_344	VSS_416	AR4
V26	VSS_345	VSS_417	AU4
BD35	VSS_346	VSS_418	AW4
CE7	VSS_347	VSS_419	BA6
V27	VSS_348	VSS_420	BC4
BD36	VSS_349	VSS_421	BE4
CF11	VSS_350	VSS_422	BE8
V3	VSS_351	VSS_423	BA4
BE10	VSS_352	VSS_424	BD4
CF14	VSS_353	VSS_425	BG4
V30	VSS_354	VSS_426	CJ2
BE28	VSS_355	VSS_427	CJ3
CF19	VSS_356	VSS_428	AM5
V33	VSS_357	VSS_429	CM4
BE29	VSS_358	VSS_430	AC5
CF2	VSS_359	VSS_431	AG5
V36	VSS_360	VSS_432	CR6
BE3	VSS_361	VSS_433	

WHL-U42_BGA1528

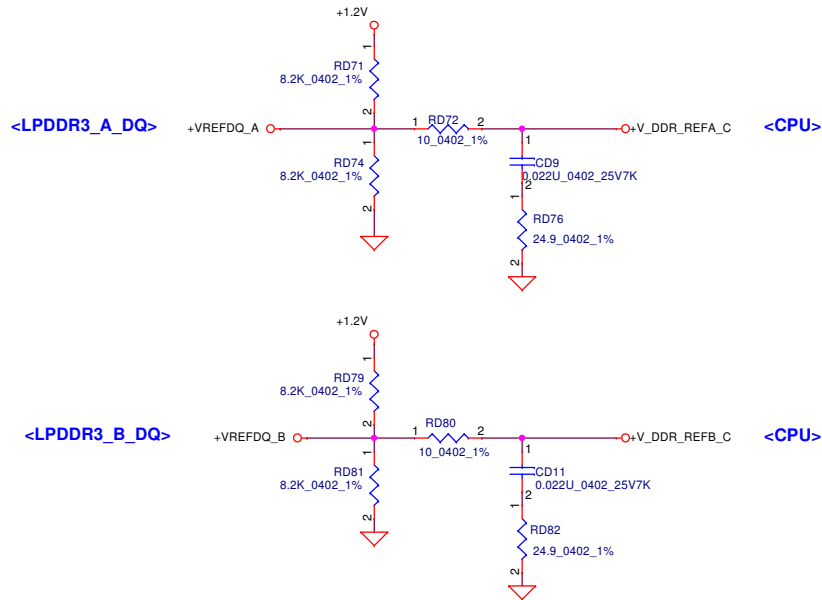
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2017/5/3		2017/6/2		LA-G651P	
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Date: Friday, May 18, 2018				Sheet 16 of 52	

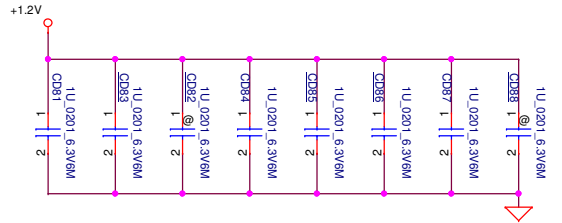
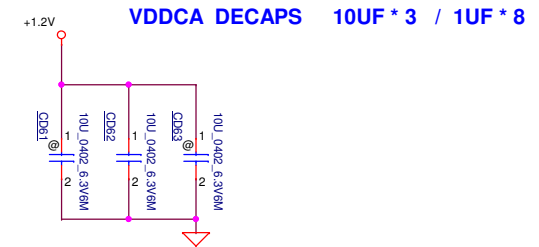
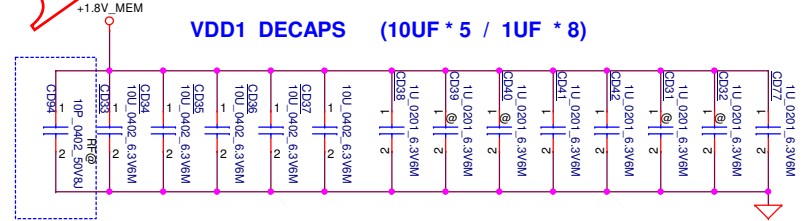
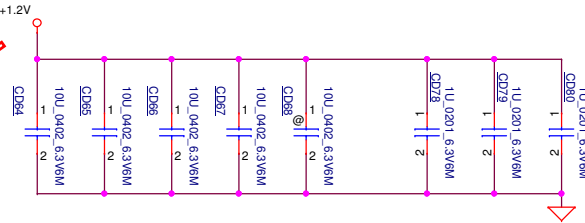
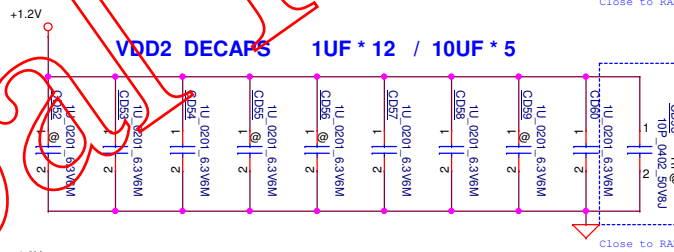
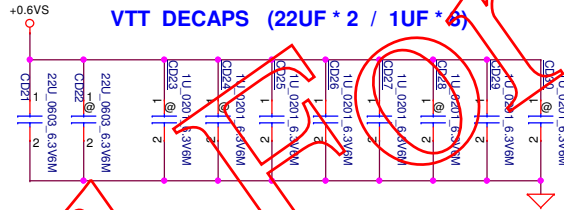
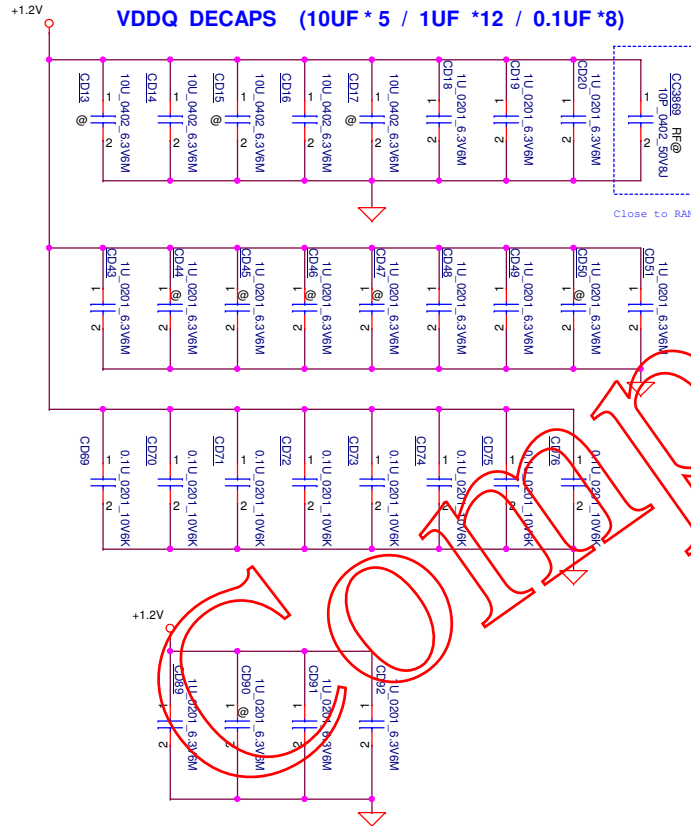


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UC1.G3
UC1.G4    NC for WHL/CNL
UC1.C34   Connect to GND for CFL-U43e
```

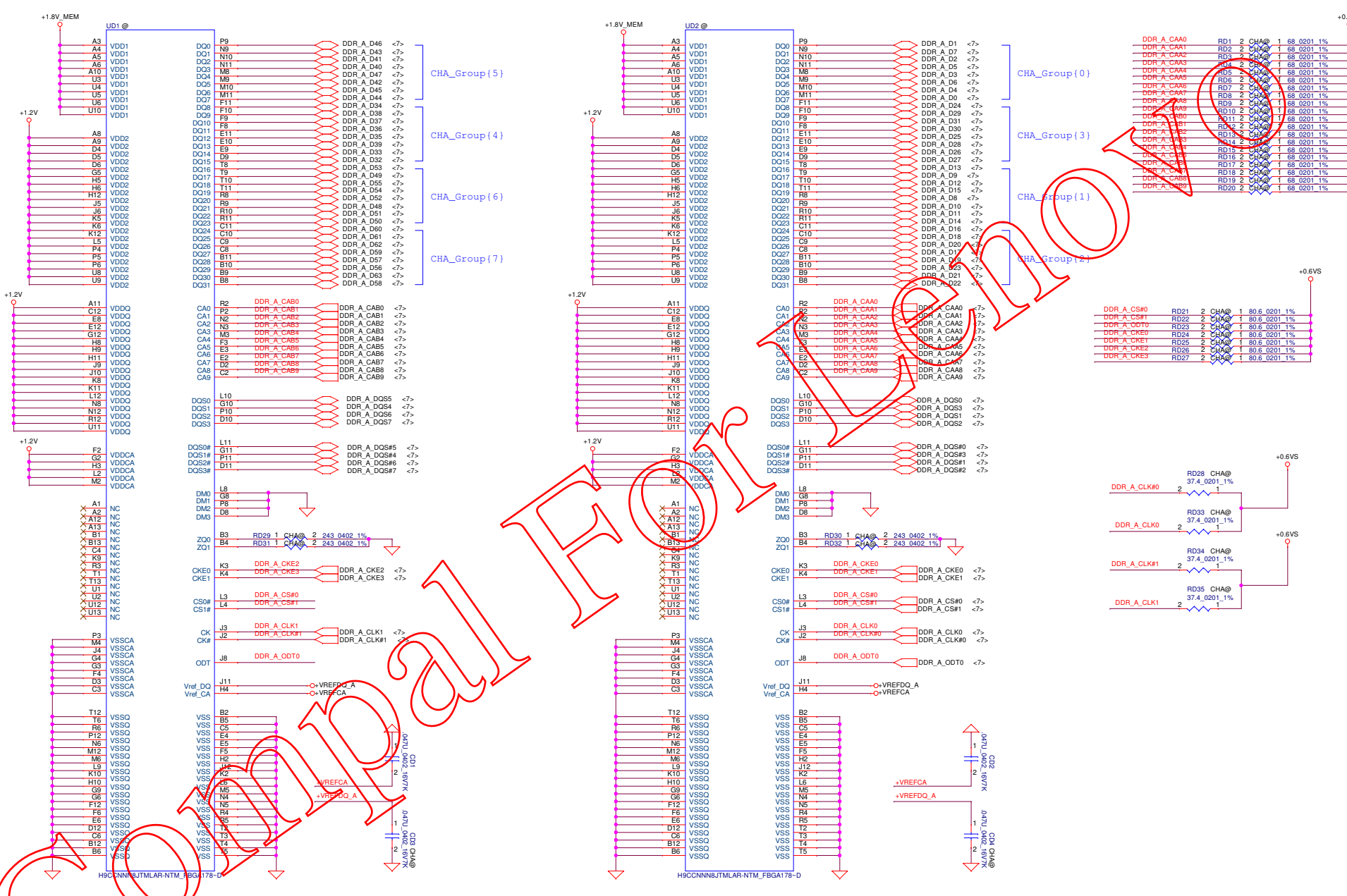
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				Date:	Friday, May 18, 2018 Sheet 17 of 52



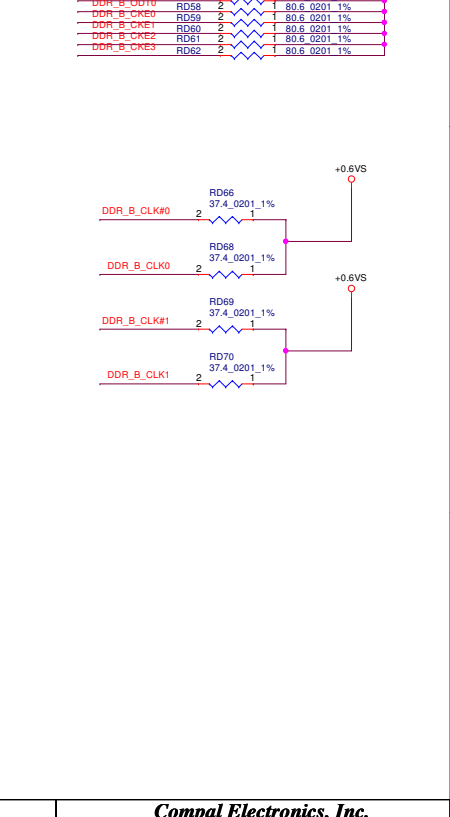
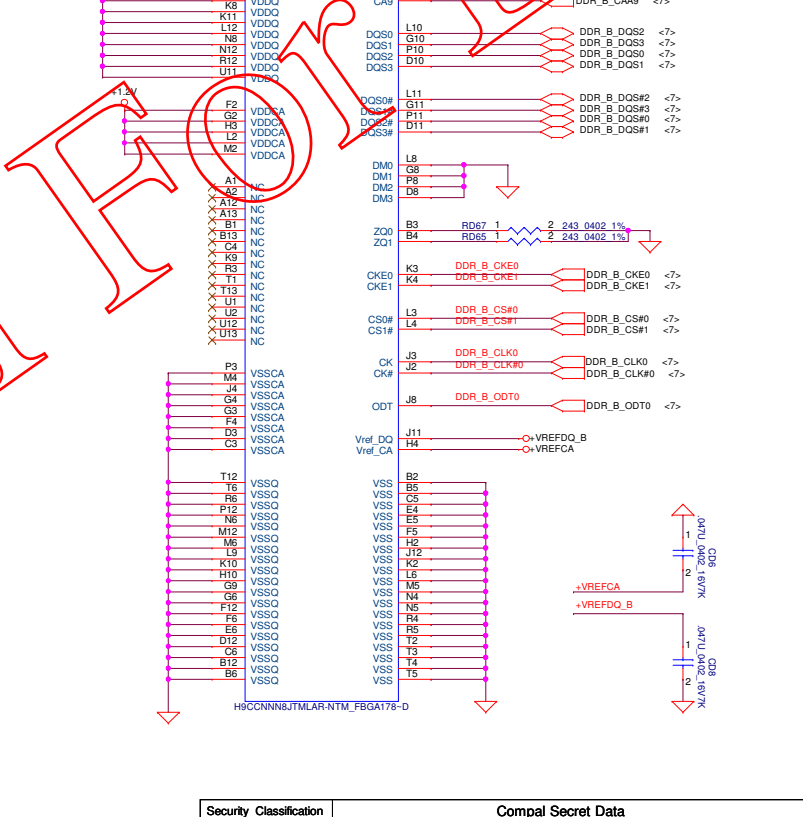
Update Cap Q'ty to follow Intel 561280_KBL_UY_PDG_Rev2_0



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		LA-G651P		0.2	
Date		Friday, May 18, 2018		Sheet 18 of 52	



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Size	Document	Number	Rev	Customer	
		LA-G651P	0.2	Date: Friday, May 18, 2018	
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					LA-G651P	0.2	
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PCIE CLK

PCIE X4 Bus

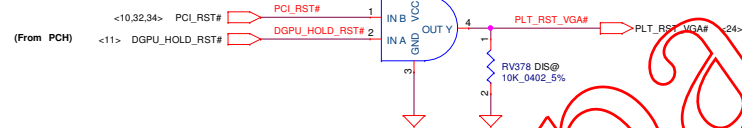
- <10> CLK_PCIE_P0
<10> CLK_PCIE_N0
<12> PCIE_CRX_DTX_P13
<12> PCIE_CRX_DTX_N13
<12> PCIE_CTX_C_DRX_P13
<12> PCIE_CTX_C_DRX_N13
<12> PCIE_CRX_DTX_P14
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<12> PCIE_CTX_C_DRX_N16

PLT_RST_VGA#
CLKREQ_PCIE#0_R

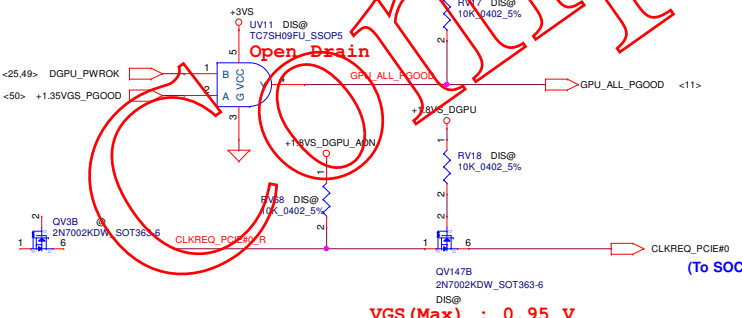
Near U1

Reset Control

1.8V AND GATE



CLK_REQ

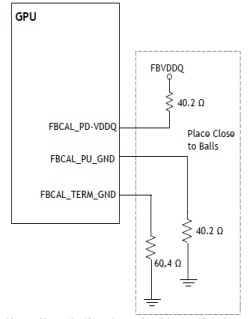
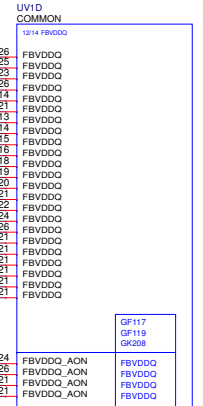
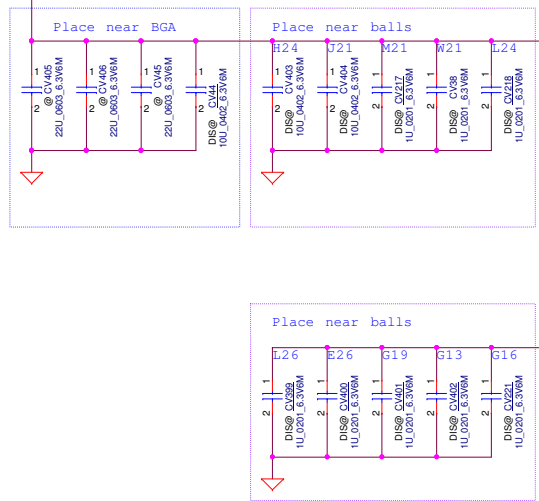


VGS(Max) : 0.95 V

Compal Electronics, Inc.

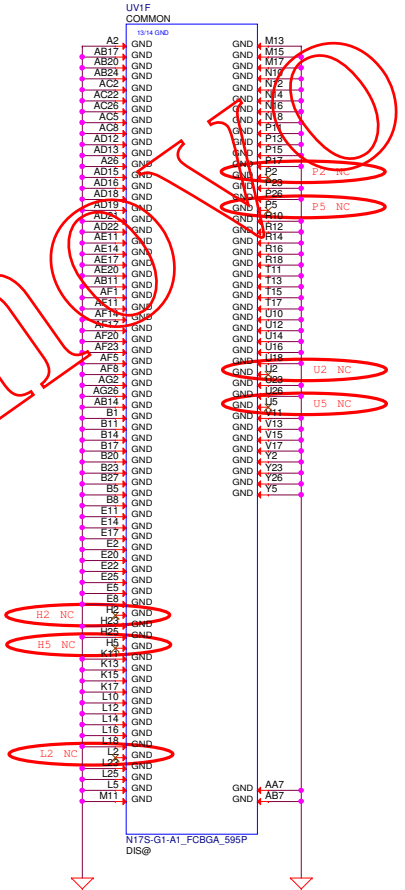
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+1.35VS_VRAM



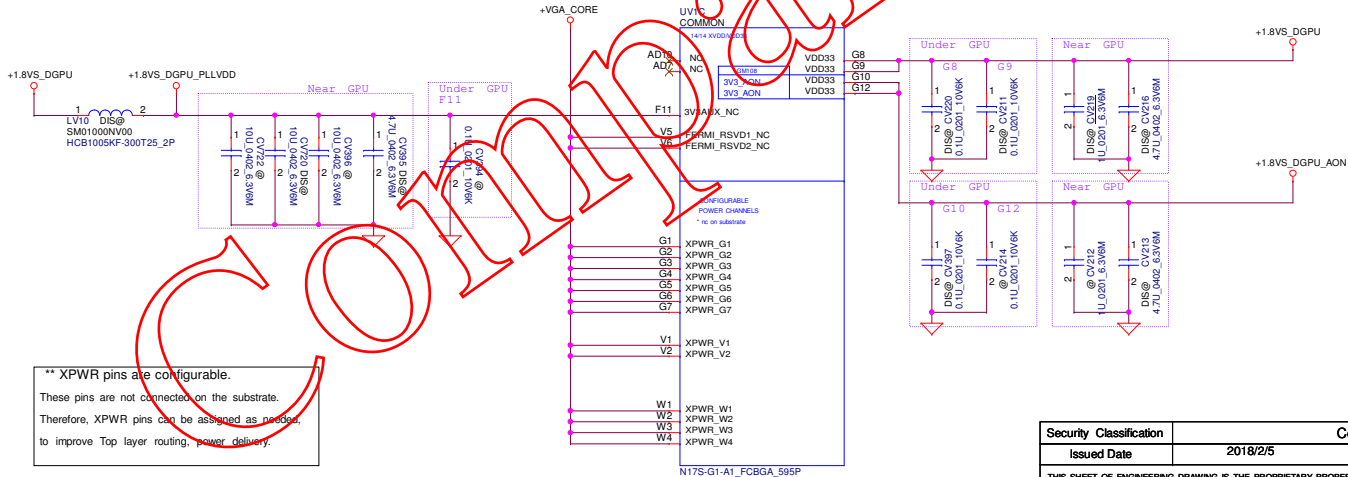
Note: Use only 1% resistors for driver calibration

GPU Decoupling CAPs @ Power Page



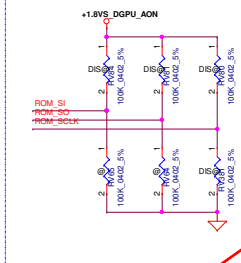
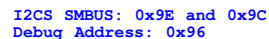
Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBVDDQ (GPU side) ¹	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
GPCPLL_AVDDx	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Q bead (0603 max ESR 0.01 Ohm)
XS_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 22uF (0805)
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	1 X 4.7uF (0402)



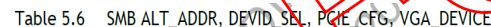
Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.



Row Index	Strap Pins <small>see Note</small>			Resulting SORX_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	X	disabled	disabled	disabled	disabled
	X	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

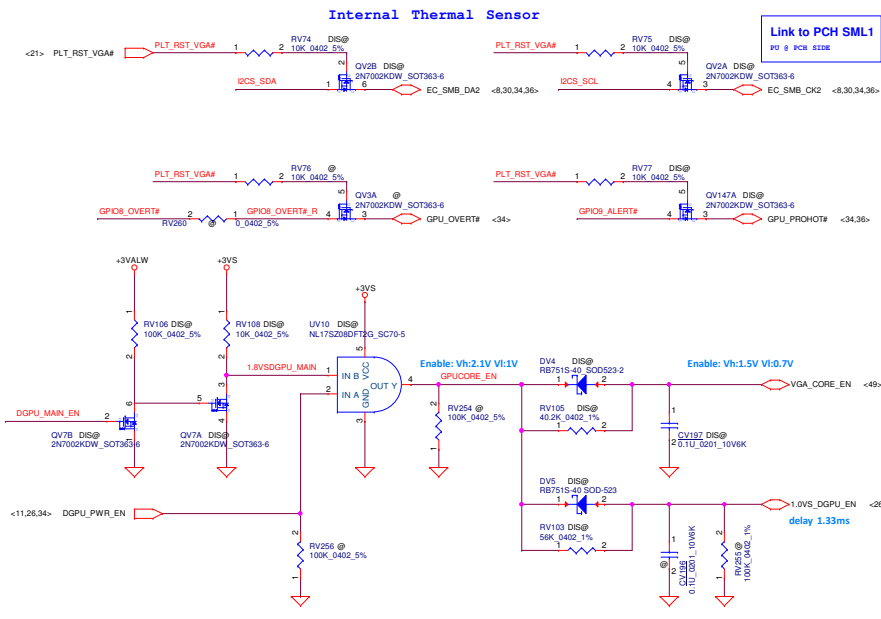
Row Index	Strap Pins <small>see Note</small>			Resulting SORX_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	X	disabled	disabled	disabled	disabled
	X	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			



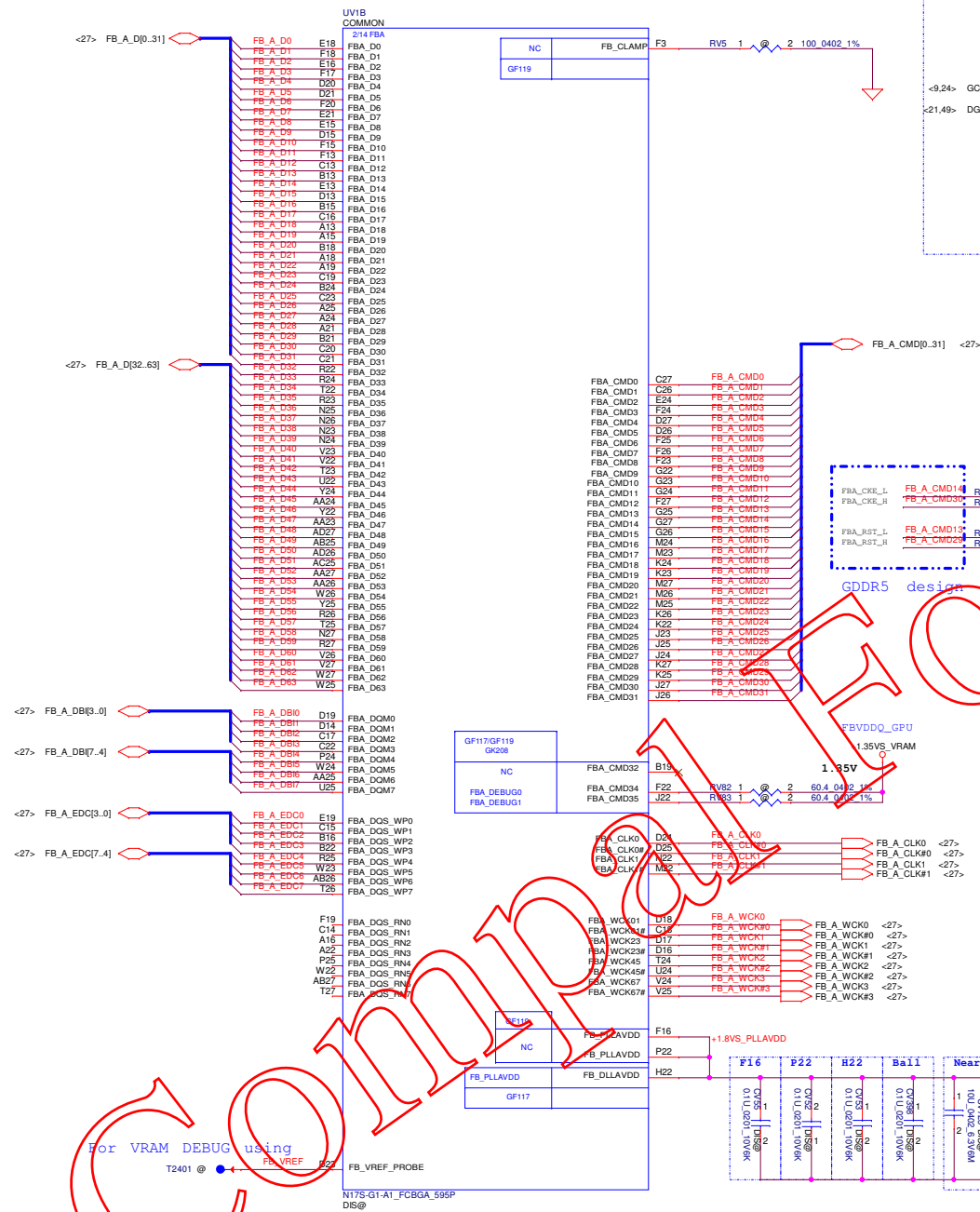
Strap Pins ^{Note 1}			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

Memory Density	Allowed Memory Configuration	FVBD/QQ	Vendor	Manufacturer Part Number	Die Revision	Stray	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G6825FB-HC28	B die	0x0	7 Gbps	N/A	N/A	Production ready
			Samsung	K4G6825FB-HC25	B die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver*
			Micron	MT51J256M32HF-70A	A die	0x1	7 Gbps	N/A	Full	Production ready
			Hyxtron	MT51J256M32HF-80A	A die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver*
			Hynix	H5G68H24MJR-R0C	A die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5G68H24MJR-R4C	A die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver*
			Micron	MT51J256M32HE-70A	B die	0x5	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80B	B die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver*
			Hynix	H5G68H24AJR-R0C	A die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5G68H24AJR-R2C	A die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver*

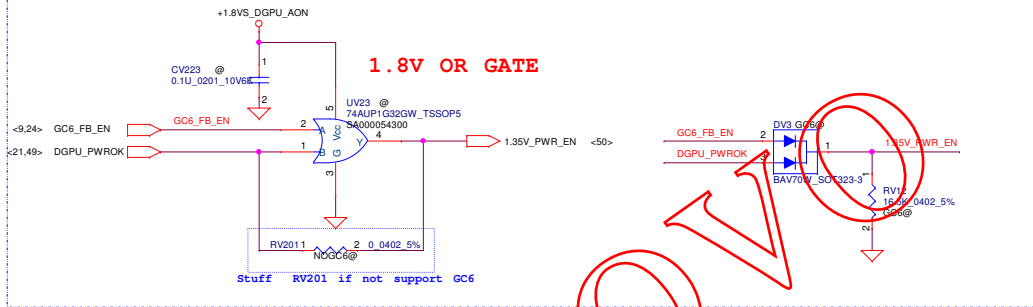
RAM_CFG	X76	STRAP2	STRAP1	STRAP0		
0x00 (LL) S2G	ZZZ X76V@	RV388 S2G@	RV390 S2G@	RV383 S2G@	UVE M2G@ SA00009D10	UV7 S2G@ SA00009D10
0x01 (LLH)						
0x02 (LHL)						
0x03 (LHH)						
0x04 (RL) M2G	ZZZ X76V@	RV382 M2G@	RV390 M2G@	RV383 M2G@	UVE M2G@ SA00009T160	UV7 M2G@ SA00009T160
0x05 (RLH) H2G	ZZZ X76V@	RV383 H2G@	RV390 H2G@	RV384 H2G@	UVE H2G@ SA00009U150	UV7 H2G@ SA00009U150
0x06 (RHL)						
0x07 (RHR)						
0x08 (LLM)						



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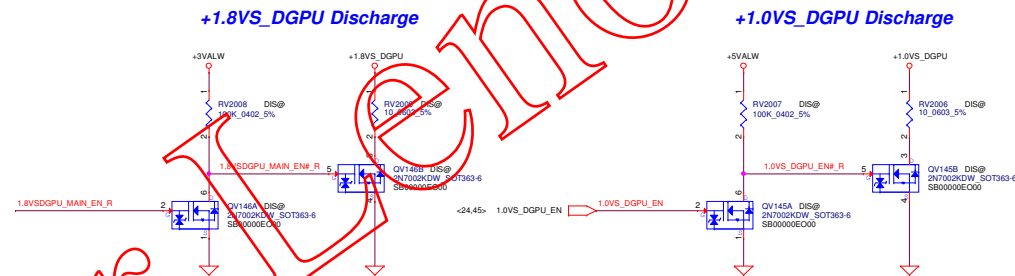
For GC6



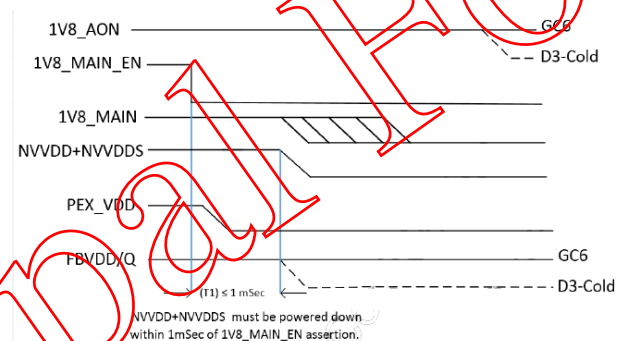
From DG-07158-001 v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

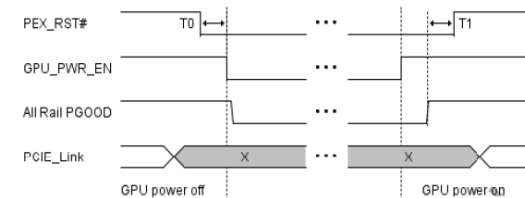
Two copies of the clock enable signal (CKE



Power-Down Sequence

[illegible]

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms



Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Figure 8.4 Cold Reset Sequence Requirement for Optimus

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				Issued	26 of 50

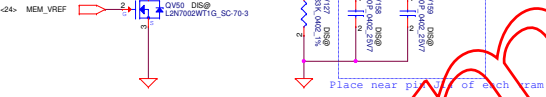
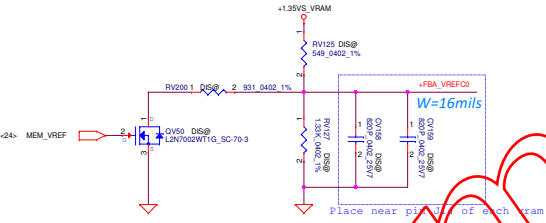
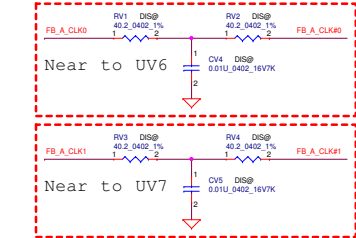
Memory Partition A

Table 7-4. GDDR5 Mode H Mapping

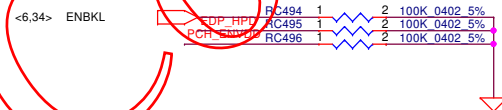
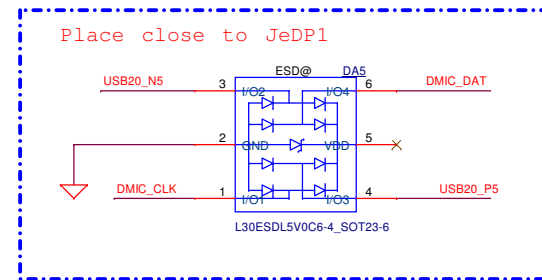
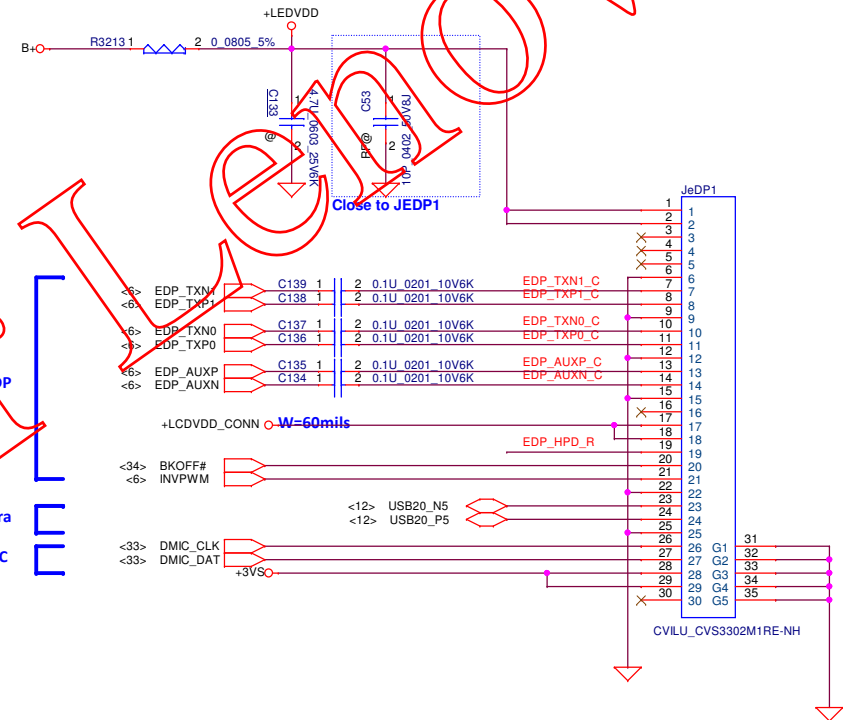
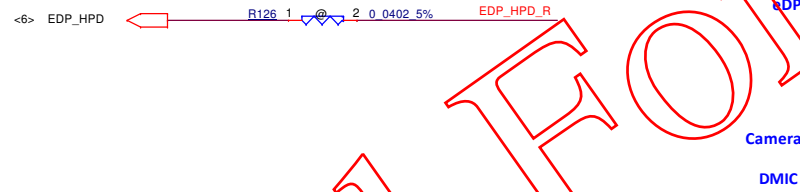
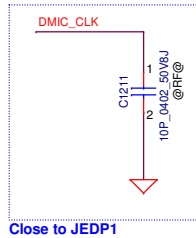
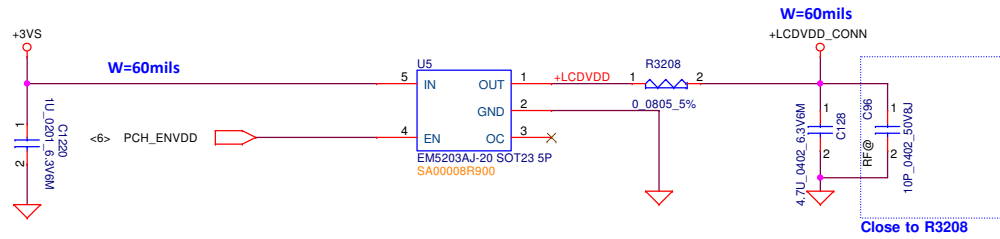
GB2-64, GB28-64, GB48-128 Channel 0 0..31			GB2-64, GB28-64, GB48-128 Channel 1 32..63		
CMD0	C5*	CMD16	CMD17	A3_BA3	C5*
CMD1	A3_BA3	CMD17	A3_BA3	A2_BA0	
CMD2	A2_BA0	CMD18	A2_BA0	A4_BA2	
CMD3	A4_BA2	CMD19	A4_BA2		
CMD4	A5_BA1	CMD20	A5_BA1		
CMD5	WE*	CMD21	WE*		
CMD6	A7_A8	CMD22	A7_A8		
CMD7	A8_A11	CMD23	A8_A11		
CMD8	AB*	CMD24	AB*		
CMD9	A12_RFU	CMD25	A12_RFU		
CMD10	A0_A10	CMD26	A0_A10		
CMD11	A1_A9	CMD27	A1_A9		
CMD12	RA*	CMD28	RA*		
CMD13	RS*	CMD29	RS*		
CMD14	CK*	CMD30	CK*		
CMD15	CAS*	CMD31	CAS*		

GB2-64, GB28-64, GB48-128 Channel 0 to 1		
CMD32	Not used	
CMD33	Not used	
CMD34	DEBUG2	
CMD35	DEBUG1	

Notes:
1. Not available in GB2-64 and GB28-64 packages.
2. GPU debug pins not connected to UGMA; see section 7.1.13.

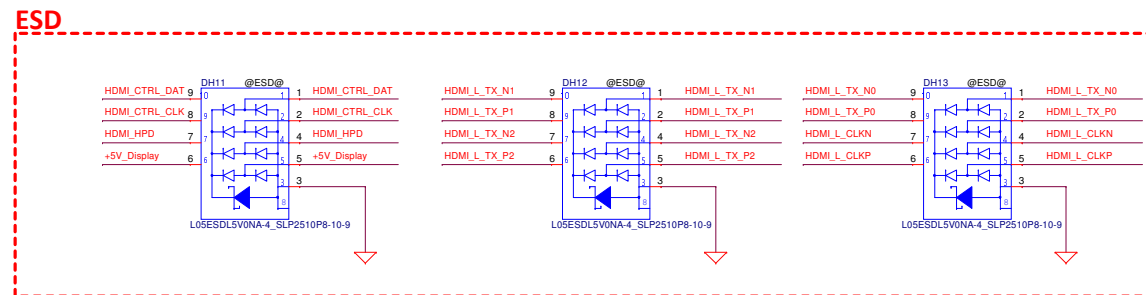
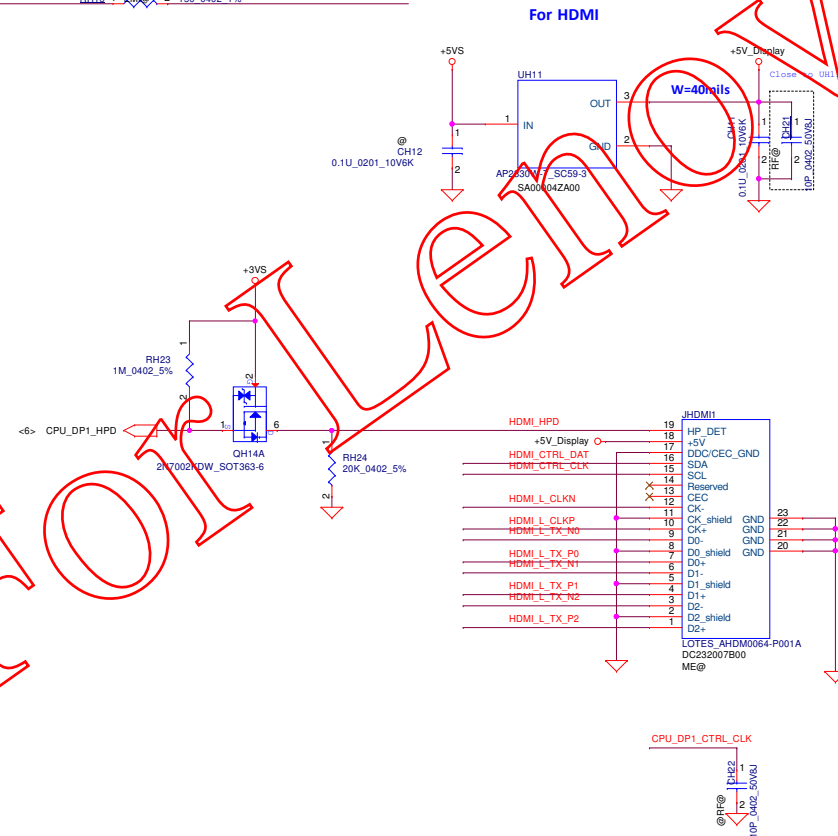
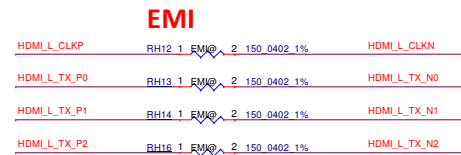
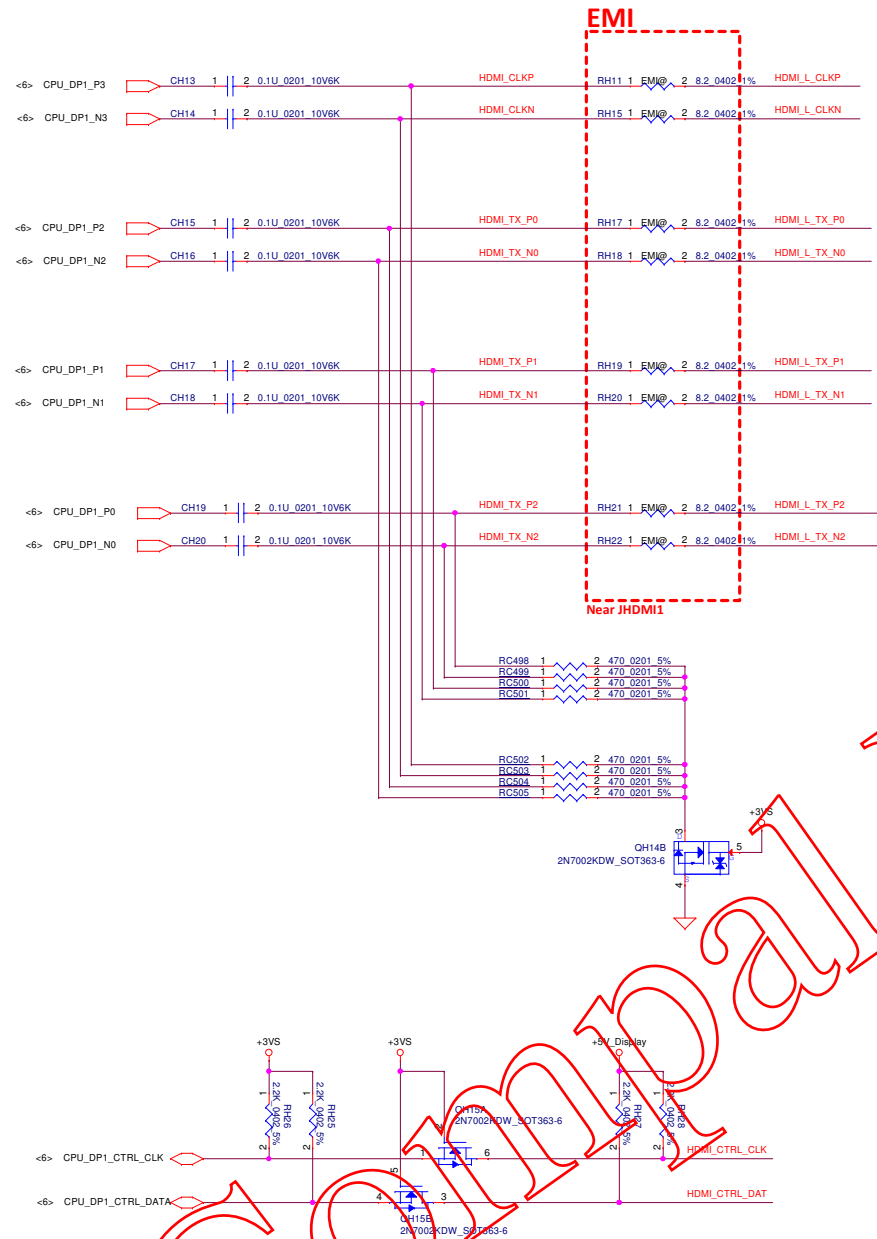


LCD Power Circuit



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						Size		Document Number		Rev	
						Custom		LA-G651P		0.2	
						Date:		Friday, May 18, 2018		Sheet 28 of 52	

HDMI



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						Date: Friday, May 18, 2018				Sheet 29 of 52	

Timing diagram showing the relationship between EC_SMB_DA2_R and EC_SMB_CK2_R signals. The diagram includes the following parameters:

- EC_SMB_DA2_R: R3239 1, 2 0.0402 5%, I2C_1_SDA <11>
- EC_SMB_DA2: R3240 1, 2 0.0402 5%, EC_SMB_DA2 <8,24,34,36>
- EC_SMB_CK2_R: R3241 1, 2 0.0402 5%, I2C_1_SCL <11>
- EC_SMB_CK2: R3242 1, 2 0.0402 5%, EC_SMB_CK2 <8,24,34,36>

[illegible][illegible]

```
Realtek
RTS5455

DB_CFG
CC1
CC2

C_TX2_1P2N
C_TX2_1N2P

C_RX2_1P2N
C_RX2_1N2P

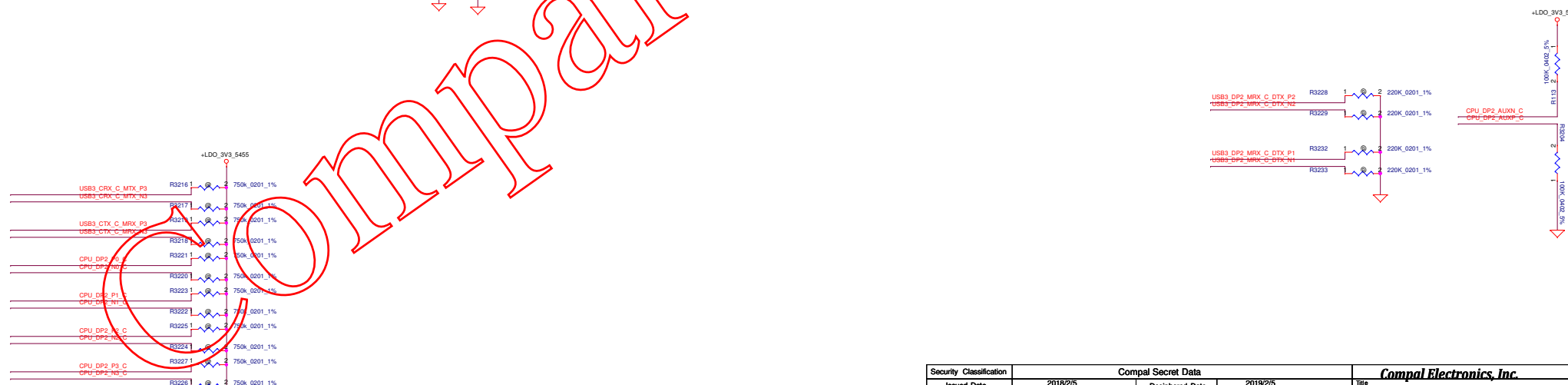
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C_TX1_1N2P

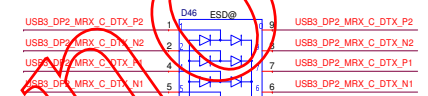
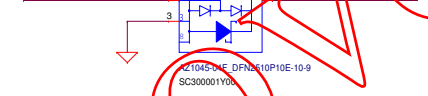
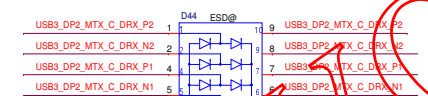
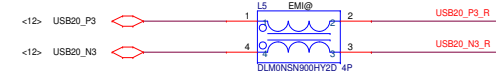
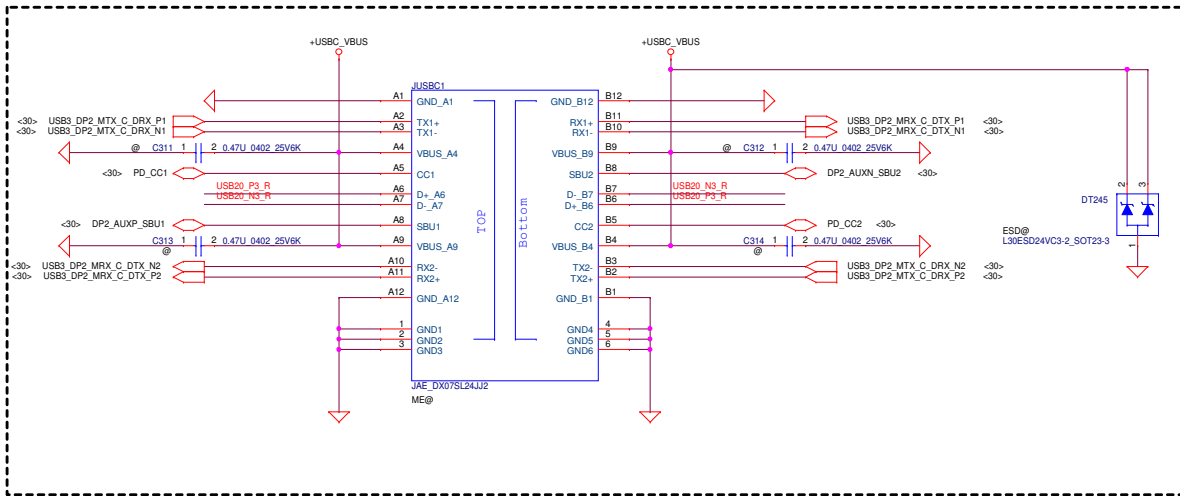
C_RX1_1P2N
C_RX1_1N2P

SBU1/MGP1
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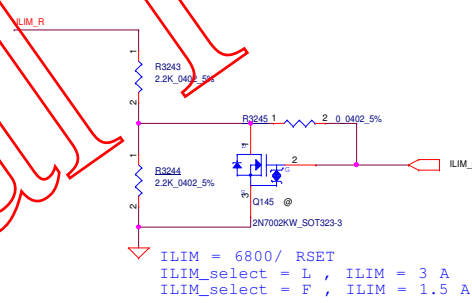
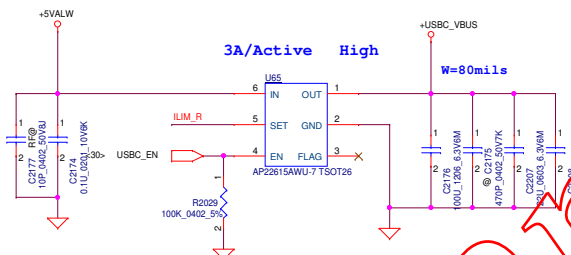
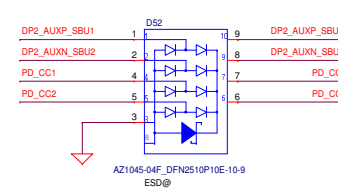
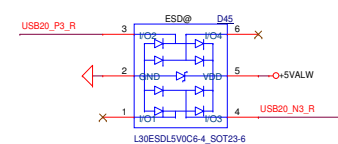
The schematic diagram illustrates the internal structure of the USB DP2 and DP1 channels. It shows the connection between the DB_CFG R157.1 and the USB_DP2_MTX_DP1 and USB_DP2_MRX_DP1 blocks. The diagram includes various components such as capacitors (C168, C169), multiplexers, and control logic. The USB_DP2_MTX_DP1 block is connected to the USB_DP2_MRX_DP1 block via a series of multiplexers and buffers. The diagram is heavily annotated with red handwritten marks, including a large 'E' and a large 'X'.

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

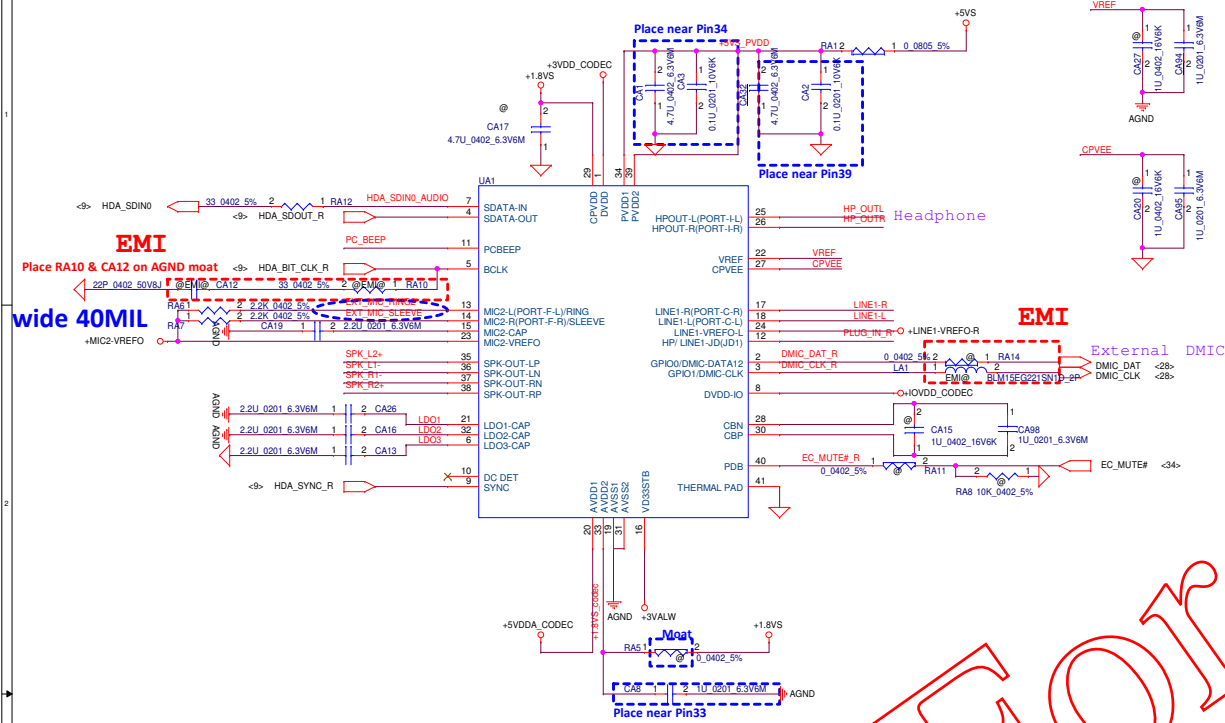




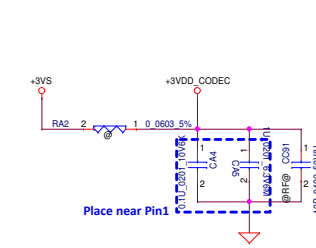
ESD for USB1 Lines and Control lines



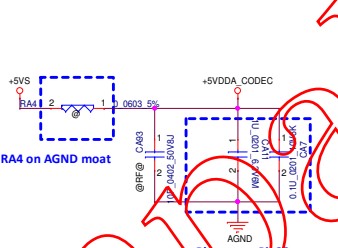
ALC3240



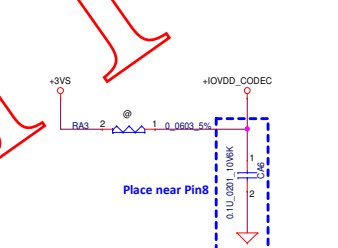
+3VS to +3VDD_CODEC



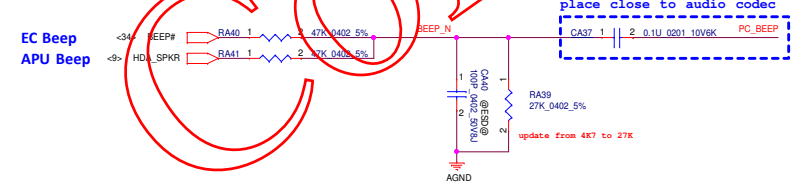
+5VS to +5VDDA_CODEC



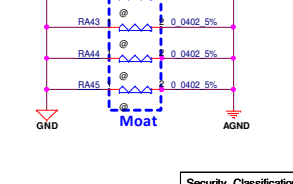
+3VS to +IOVDD_CODEC



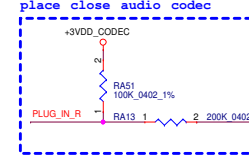
PC BEEP



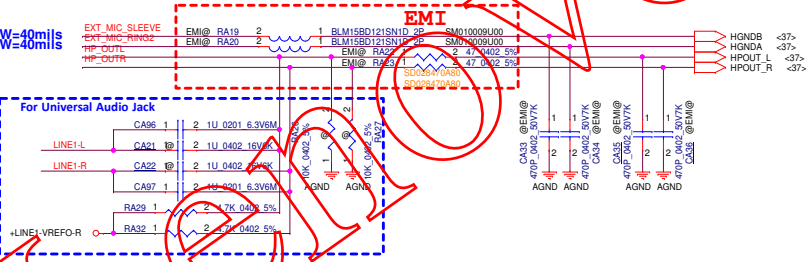
At least one R-Short short close to UA1



Head Phone Input



Audio Combo Jack



Speaker

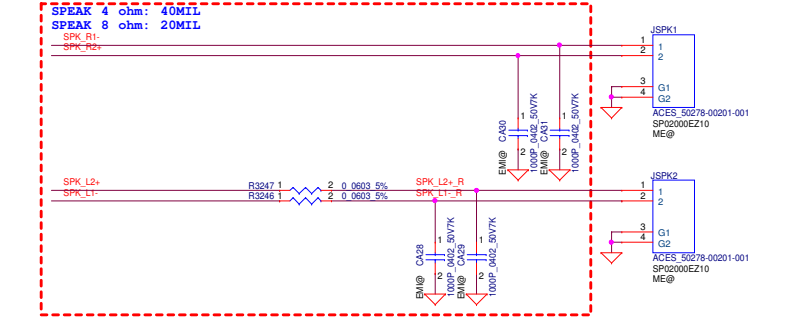
Note:

Cable Color	SPK driver Pin Definition	M/B SPK connector Pin Definition	
Black	R-	Pin1	SPK R1-
Red	R+	Pin2	SPK R2+
White	L+	Pin3	SPK L2+
Blue	L-	Pin4	SPK L1-

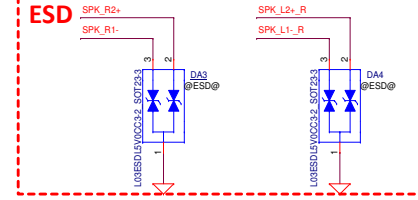
Pin 金屬面朝上

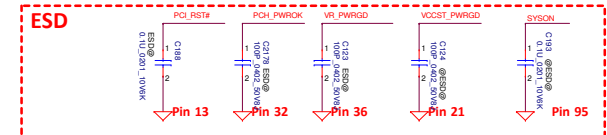
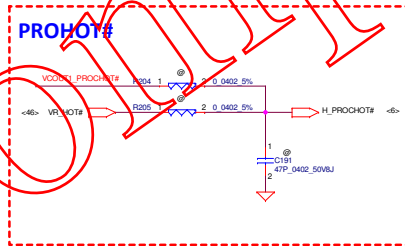
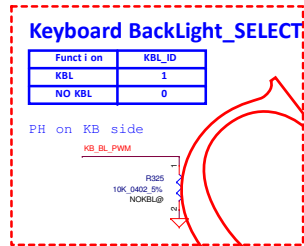


EMI

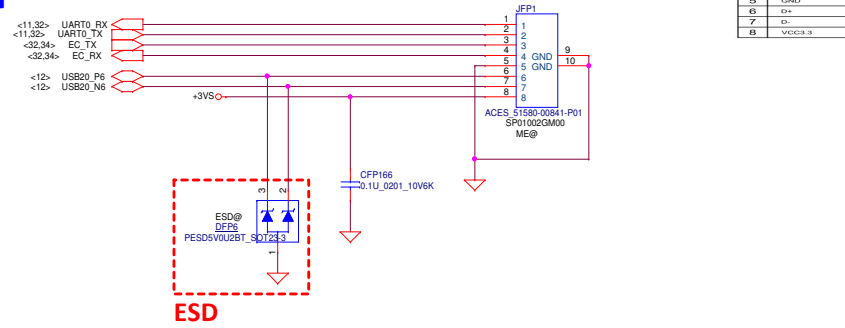


ESD protection needs to be placed near connector side

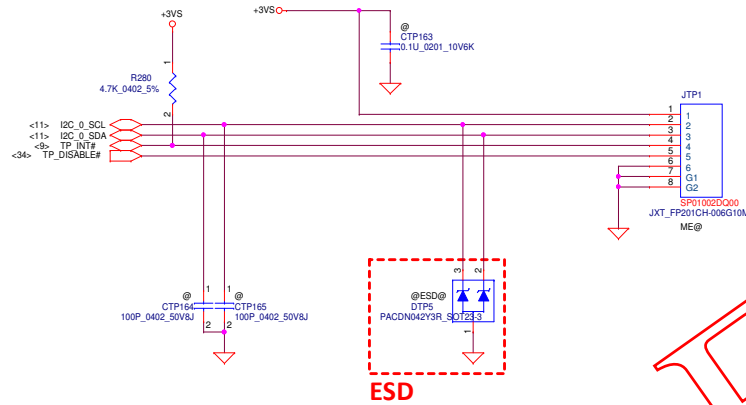




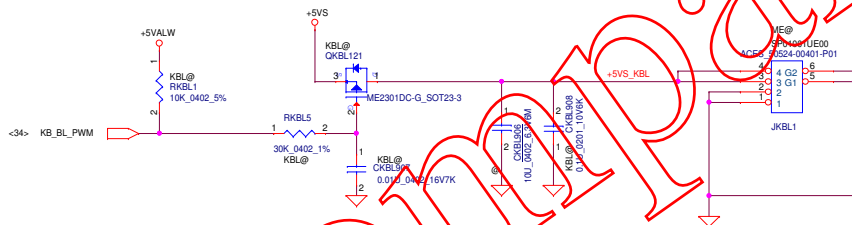
Finger printer



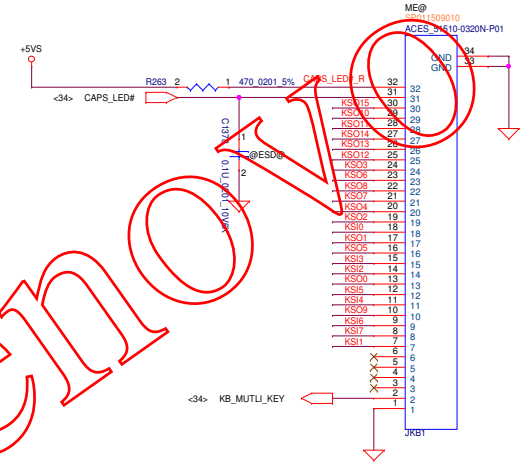
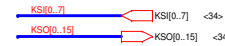
Touch Pad



Keyboard Backlight



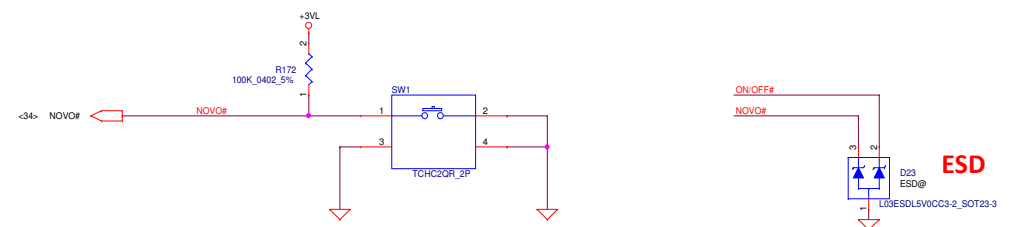
Keyboard



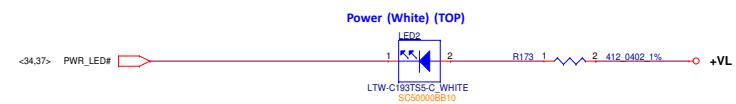
PWR Button



Novo Button

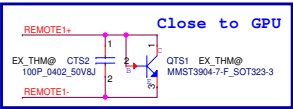
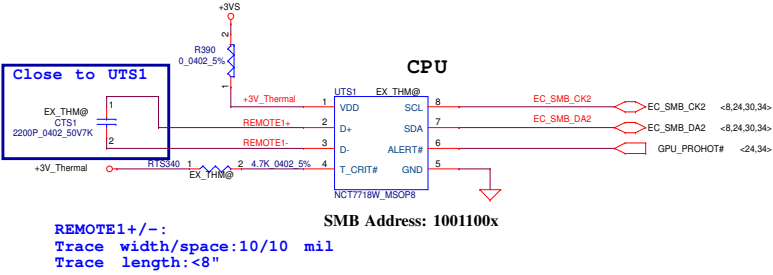


PWR LED

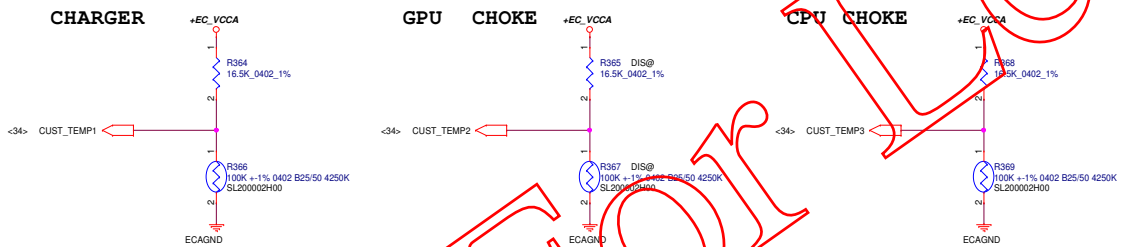


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Size C	Document Number	LA-G651P		Sheet 35 of 52
Date:	Friday, May 18, 2018			

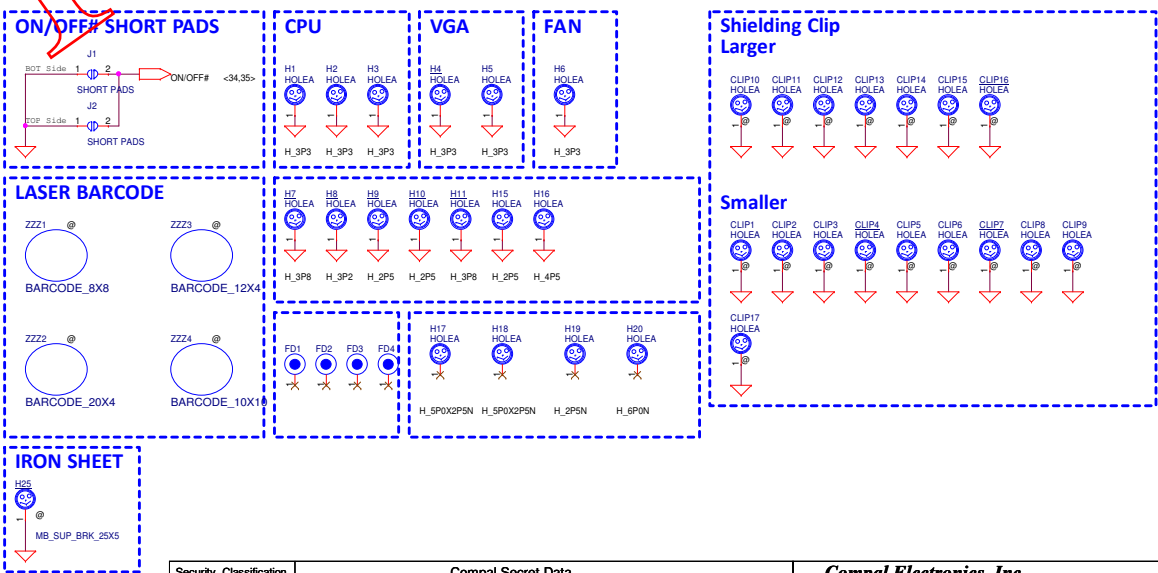
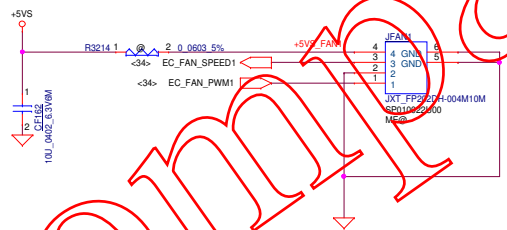
Thermal Sensor



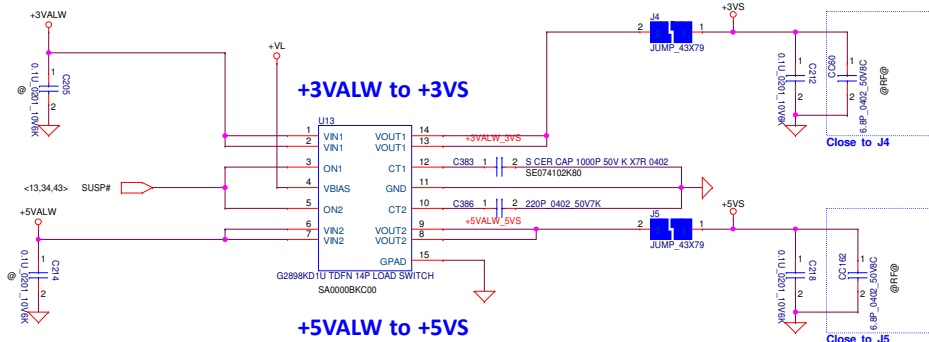
THERMISTOR



FAN

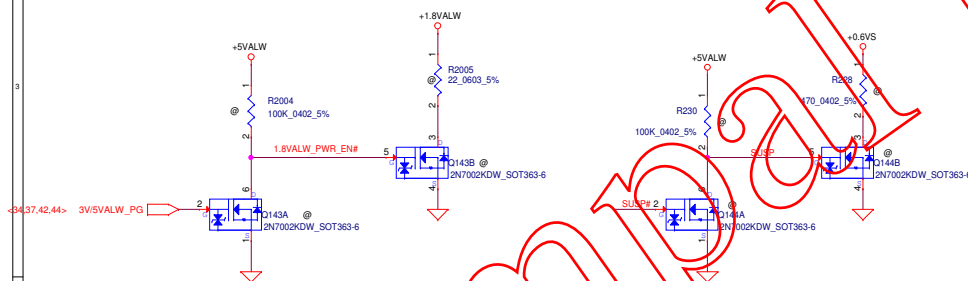


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				LA-G651P	Rev 0.2
Date: Friday, May 18, 2018				Sheet	36 of 52

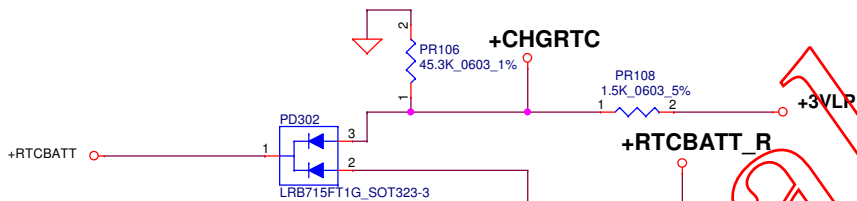
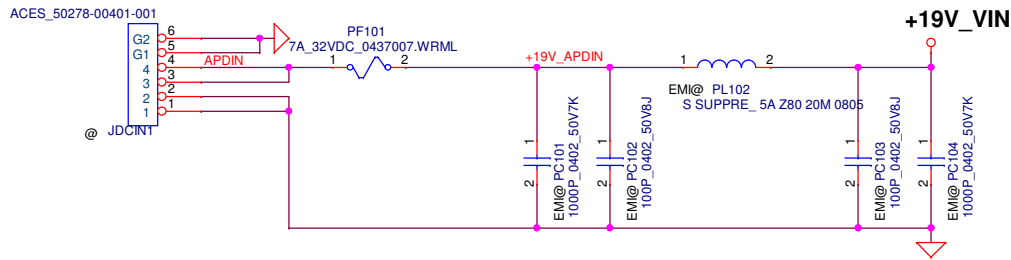


For +1.8VALW Discharge

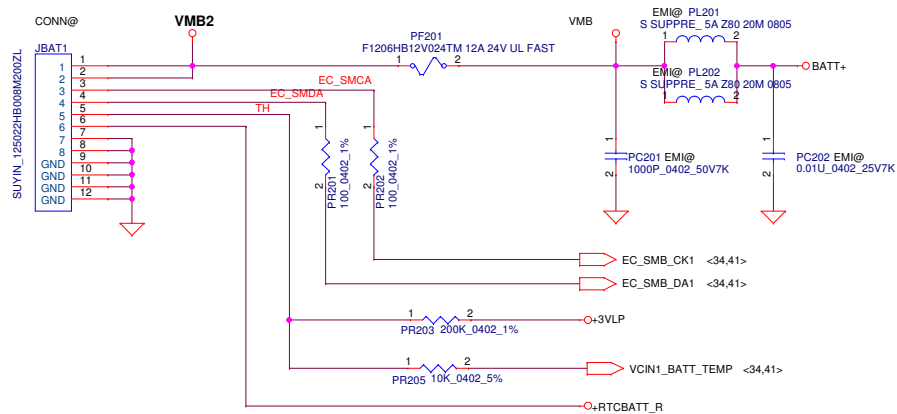
For +0.6VS Discharge



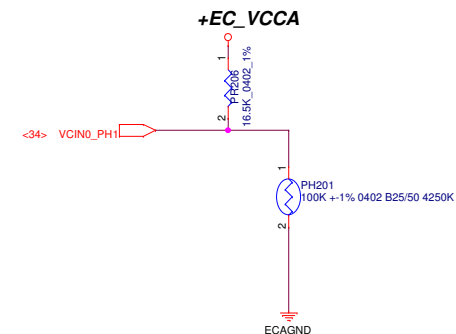
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				Size B	Rev 2.0
				Date: Friday, May 18, 2018	Sheet 39 of 54



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

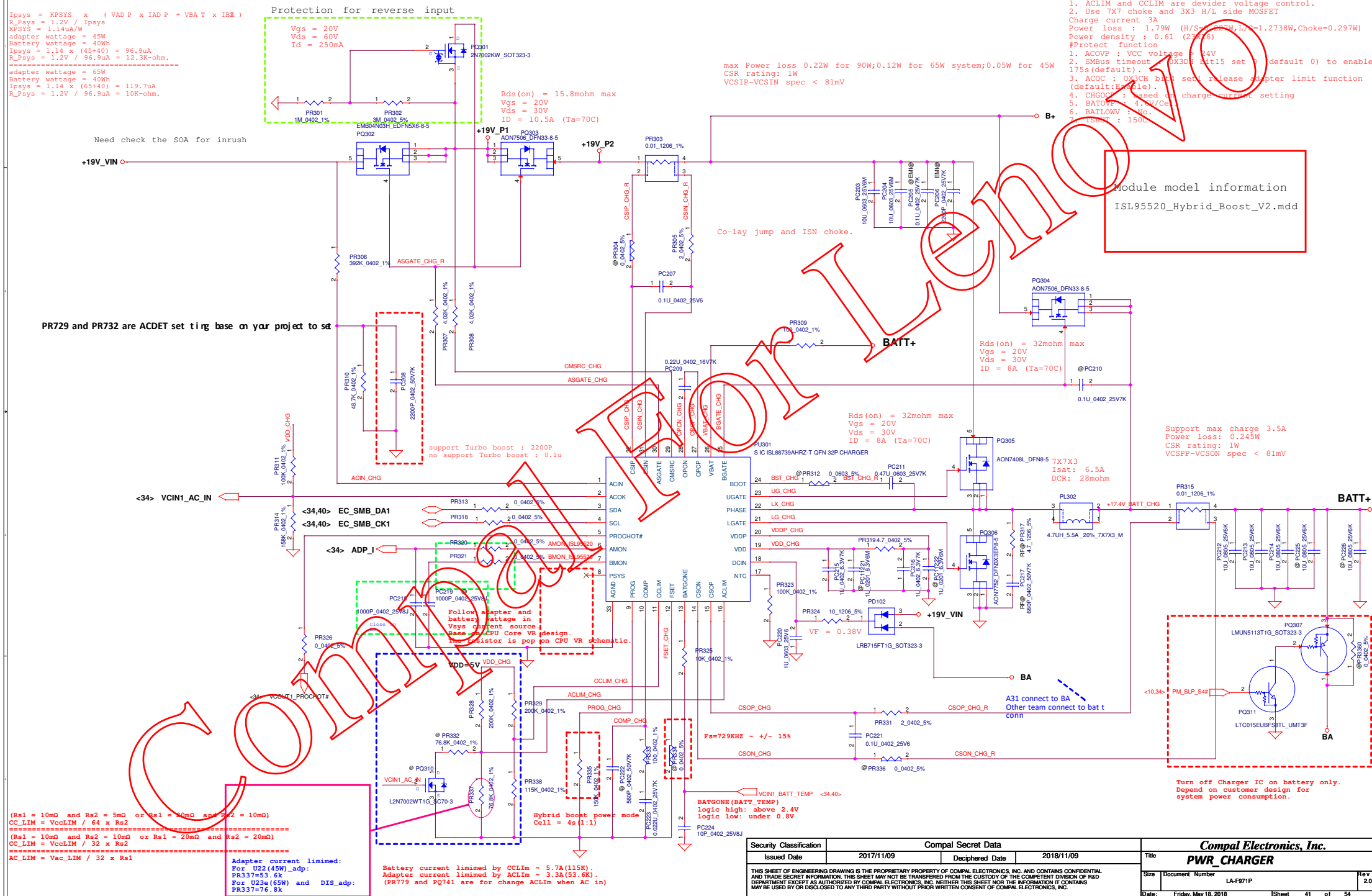


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				Date: Friday, May 18, 2018	Rev 2.0
				Sheet 40 of 54	

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**Design Notes**
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. OX3DH bit10 set 0 (default 1) to enable turbo boost
function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CLIM are divider voltage control.
2. Use 7K7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=2.27W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23876)
#Protection function
1. ACOPP : VCC voltage 0.94V
2. SWT timeout (OX3DH bit15 set 1) default 0) to enable
175s (default).
3. ACCO : OX3CH bit5 set1 release adapter limit function
(default:Enable)
4. CHOCO : based on charge current setting
5. BATOV : 4.0V/Ce
6. BATLOWV : No
7. SSBT : 150C

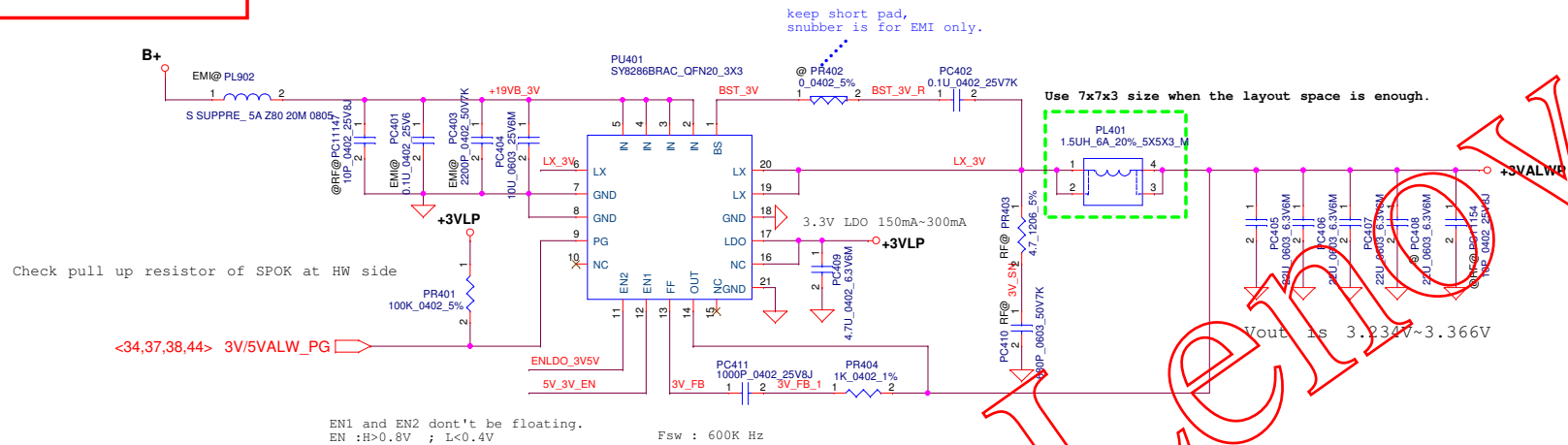
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Issued Date	2017/11/09	Deciphered Date	2018/11/09	Title	
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					LA-F971P
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				Rev	2.0

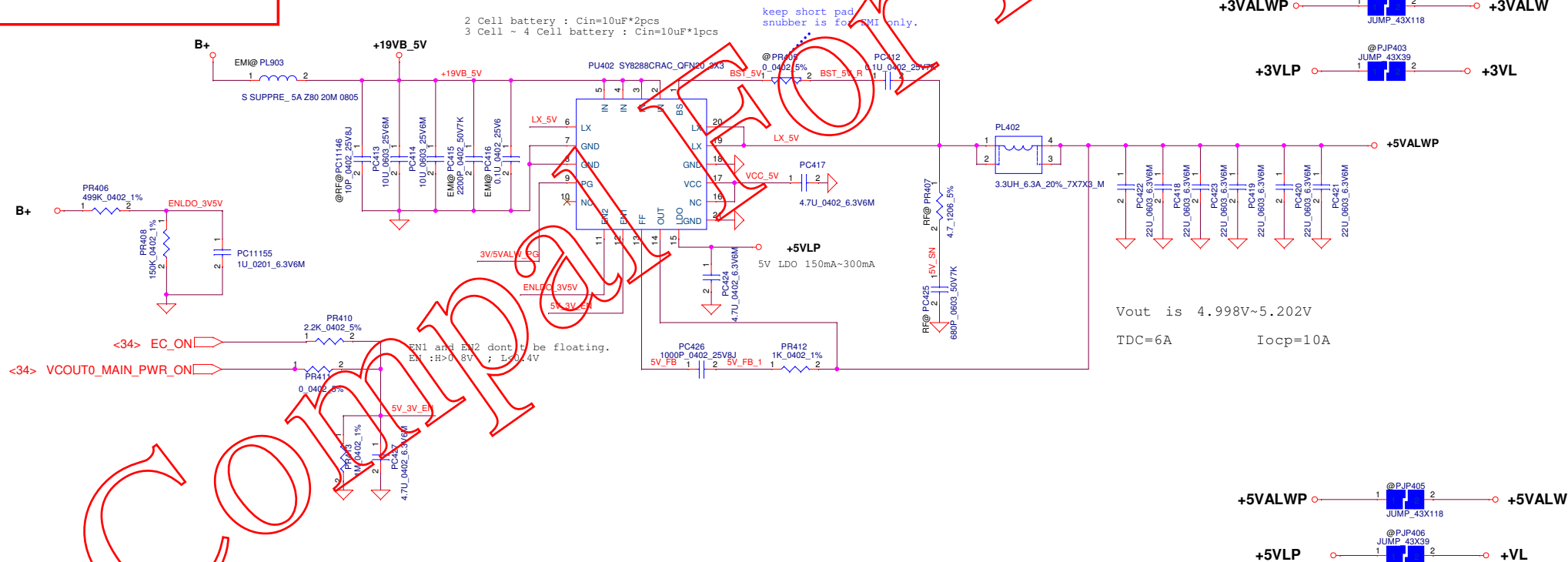
Module model information

SY8286B_V1.mdd

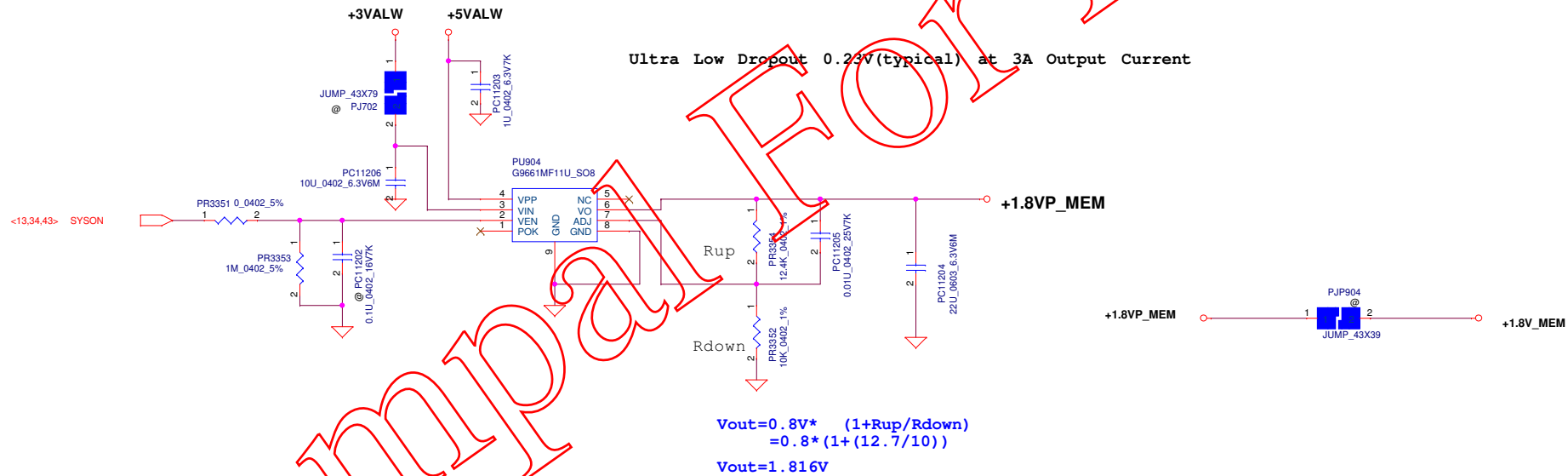
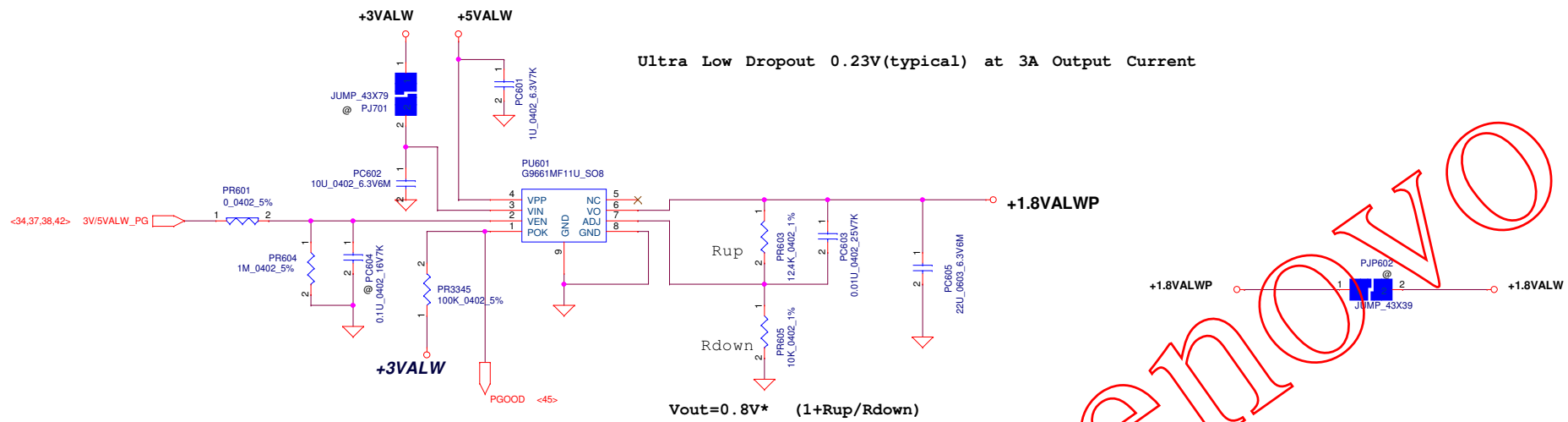


Module model information

SY8286C_V2_single.mdd
SY8286C_V2_dual.mdd



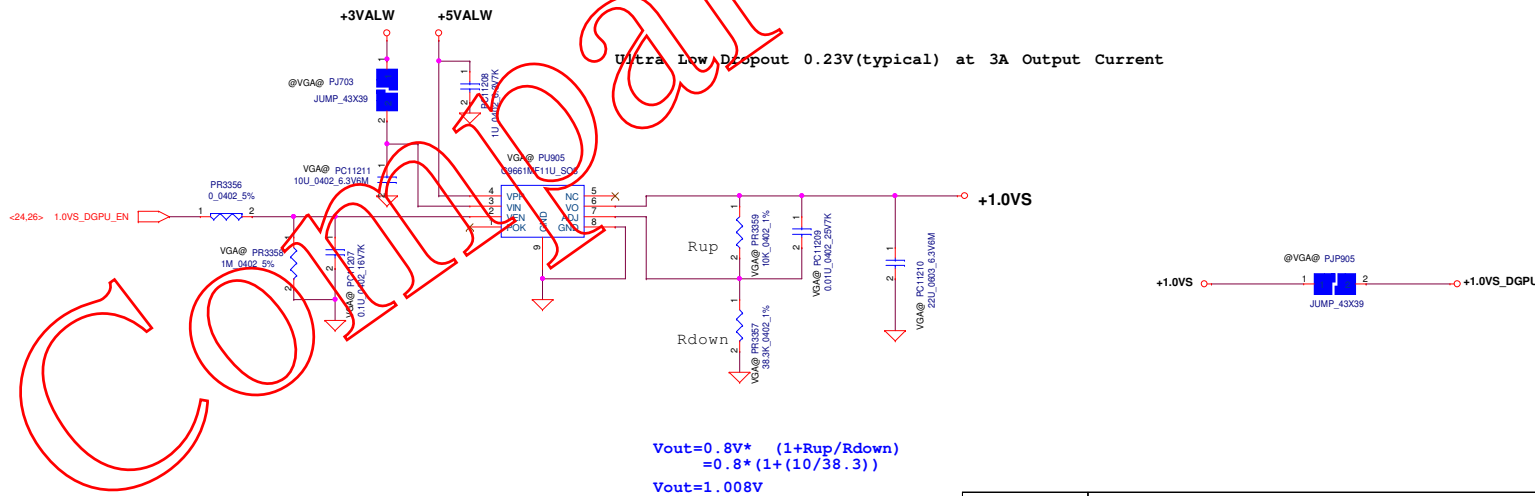
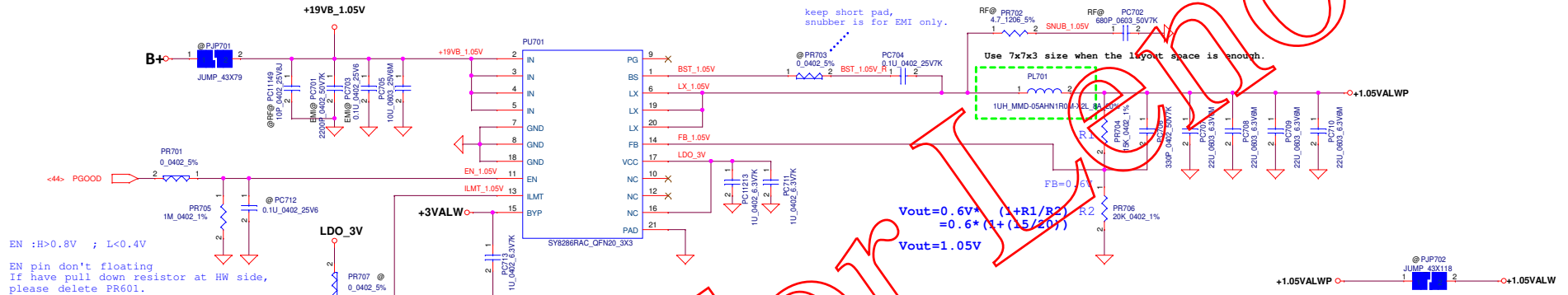
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Issued Date	2016/6/2	Deciphered Date	2017/6/2	Title	PWR- 3VALW/5VALW-SY8286B&C
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				Customer	Rev 2.0
				Date:	Friday, May 18, 2018
				Sheet	42 of 54



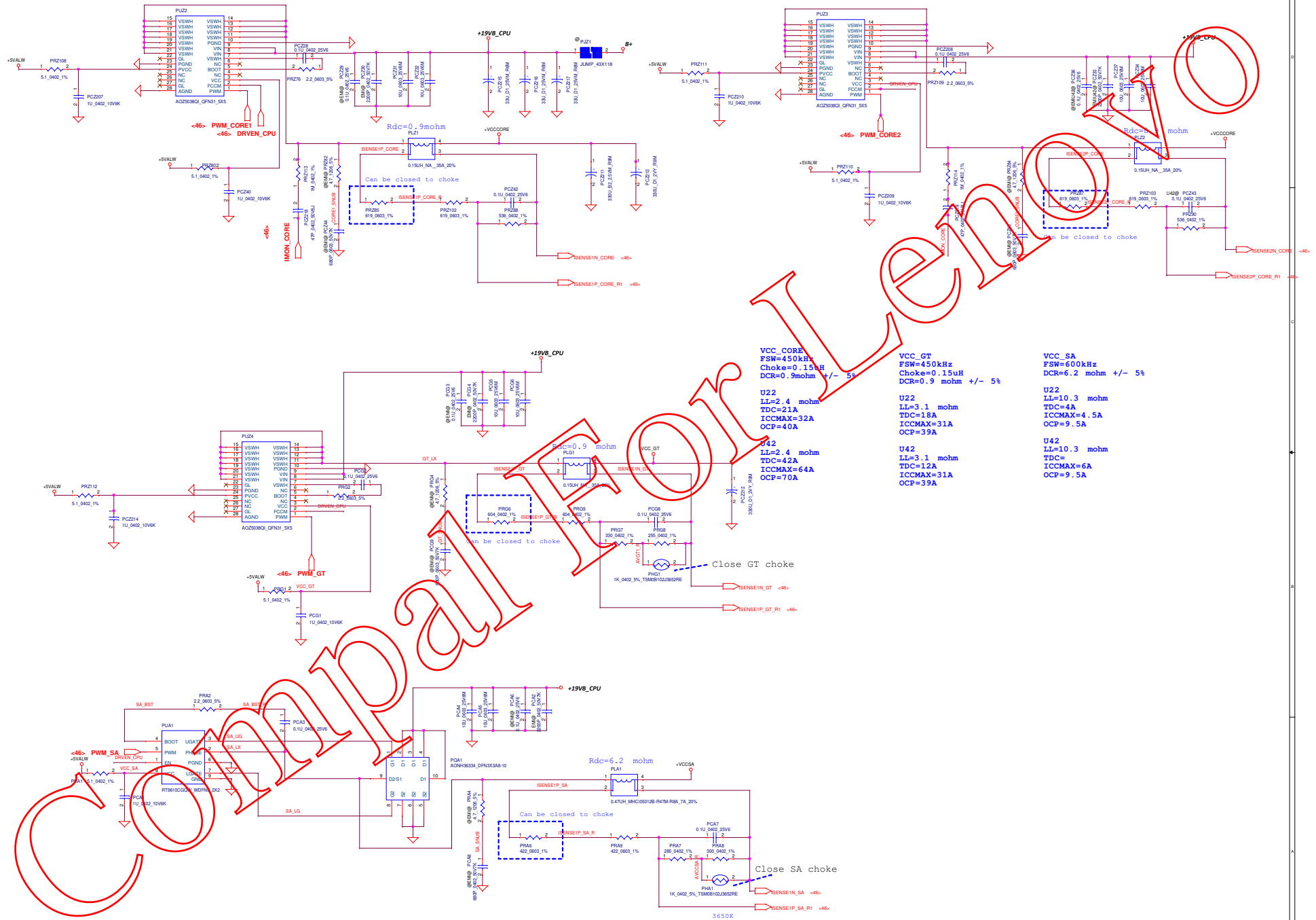
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				Size	Document Number	Rev
				Custom		2.0
				Date:	Friday, May 18, 2018	Sheet 44 of 54

Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd

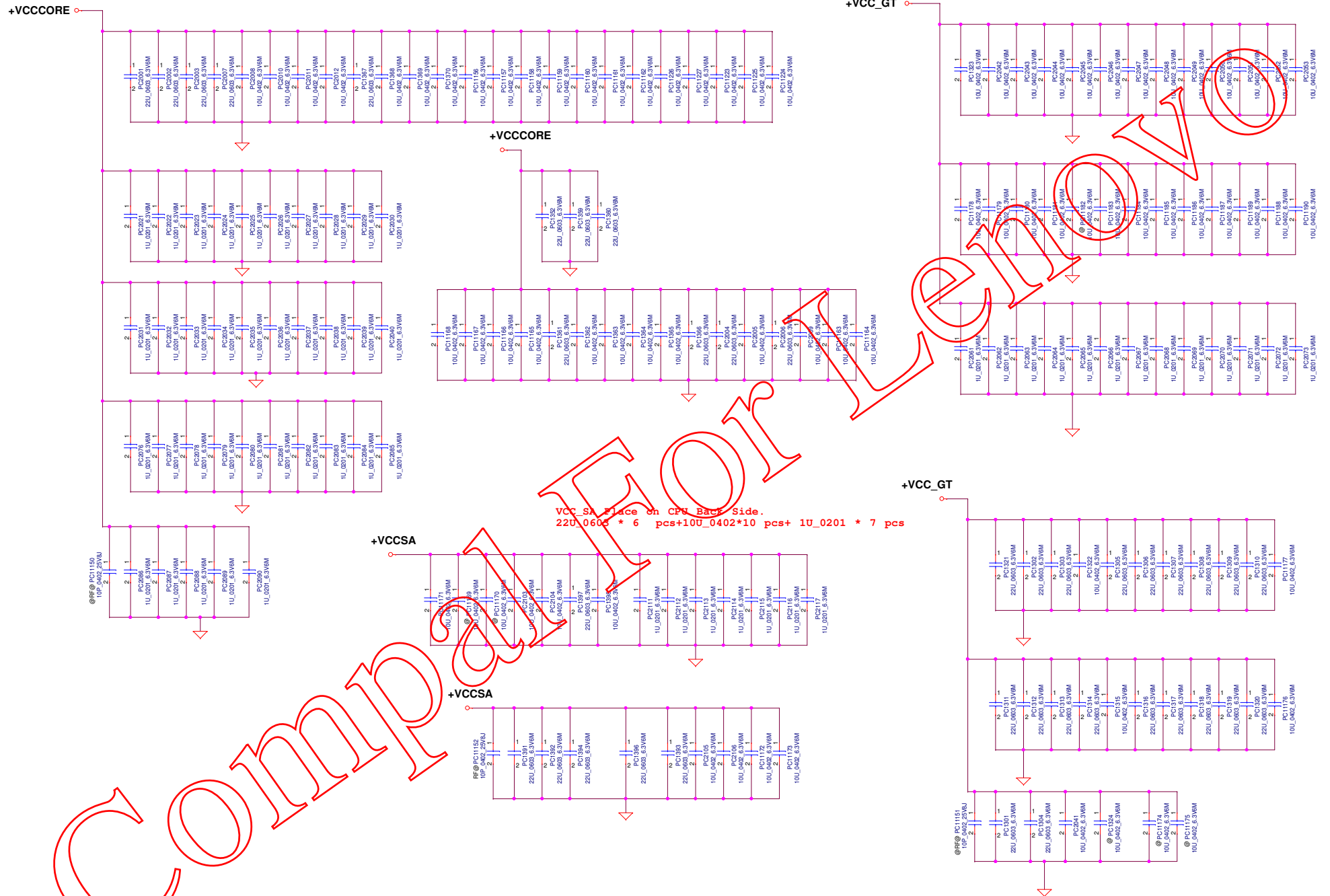


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VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 12 pcs+10U_0402*26 pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side.
22U_0603 * 20pcs+10U_0402*38 pcs +1U_0201*8pcs+ 0.47U_0201*4 pcs



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Module model information

R1, R2, R3, R4, R5, C are based on VGA type to set.

Vboot=Vvref*(Rref2/(Rref1+Rref2+Rboot))
 Rt=Rrefadj // (Rboot+Rref2)
 Vmin= Vvref*(Rref2/(Rref2+Rboot))*[Rt/(Rref1+Rt)]
 Vmax=Vvref*Rref2/(Rref1/Rrefadj)+Rboot+Rref2
 Vout=Vmin+N*Vstep
 Vstep=(Vmax-Vmin)/Nmax

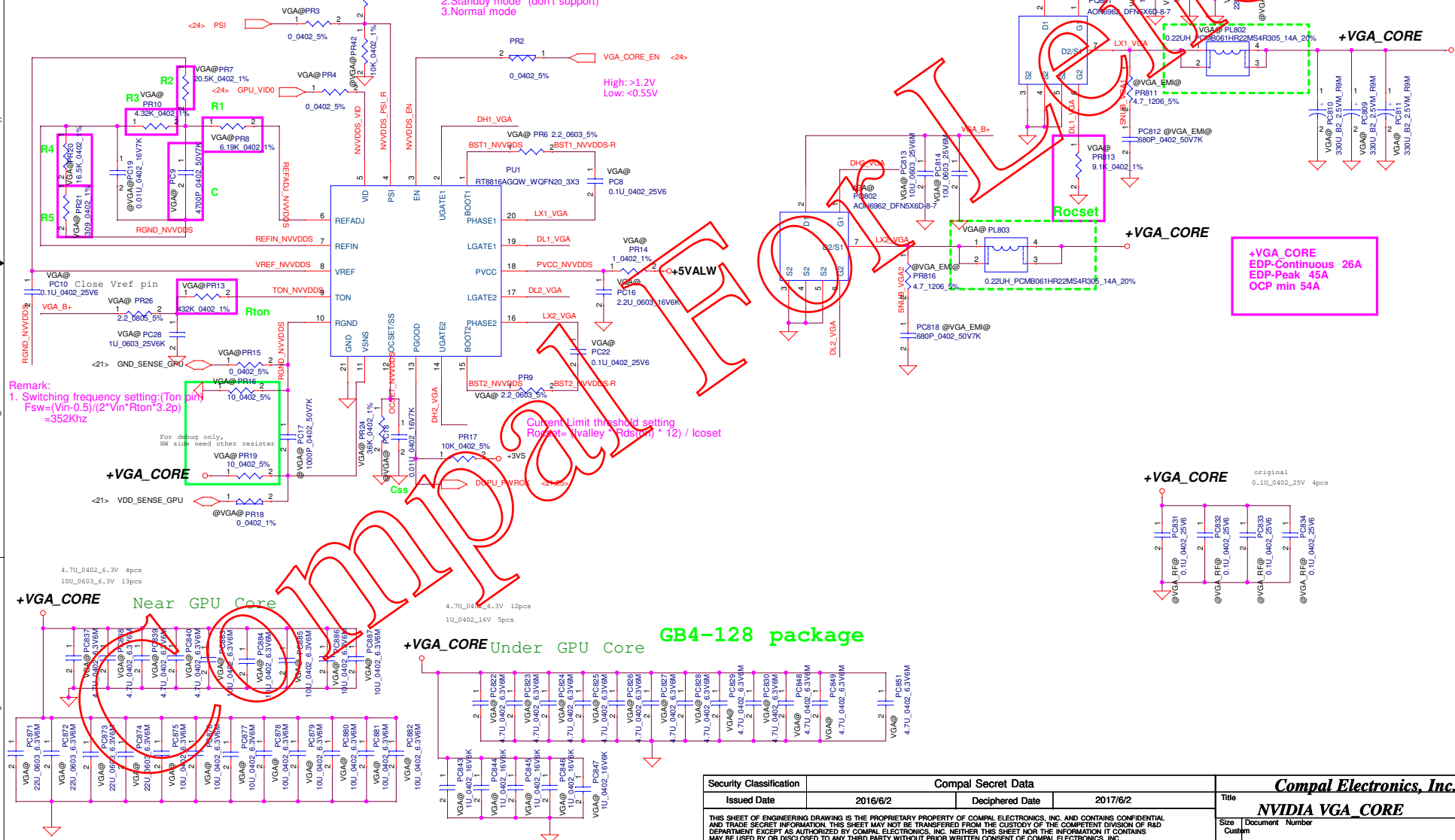
OpenVReg Configurations (PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with CCM	1.6V to 5.5V

+1.8VS_DGPU_AON

PWM VID and Output voltage control
 1. Boot mode
 2. Standby mode (don't support)
 3. Normal mode

High: >1.2V
 Low: <0.55V



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Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd

